# DATA SHEET

# General data Surface-mount ceramic multilayer capacitors

Product specification Supersedes data of 11th February 1999 2001 May 30 Rev.6





### Surface-mount ceramic multilayer capacitors

#### General data

#### **PACKING**

#### Tape on reel

Packing conforms fully with "IEC 60286-3", "EIA 481-1" and "JIS C0806" industrial standards.

Multilayer Chip Capacitors (MLCCs) are supplied on tape on reel or in bulk case. For MLCCs with a product thickness of <1 mm, paper tape is preferred. MLCCs with a product thickness of ≥1 mm, are supplied in embossed blister tape.

**CARRIER TAPE** 

Polycarbonate.

Table 1 Properties of carrier tape

PARAMETER	WIDTH				
PARAMETER	8.1 ±0.2 mm	12 ±0.2 mm			
Thickness	190 to 280 μm	240 ±20 μm			
Tensile strength at break	>60 N/mm <sup>2</sup>	>60 N/mm <sup>2</sup>			
Elongation at break	100 to 150%	100 to 150%			
Surface resistance	$>10^{12} \Omega/\text{sq}$ .	$>10^{12} \Omega/\text{sq}$ .			

COVER TAPE

Polyester (antistatic).

Table 2 Properties of cover tape

PARAMETER	WIDTH			
PANAMETER	5.5 ±0.1 mm	9.5 ±0.1 mm		
Breaking force	≥10.7 N	≥17.6 N		
Elongation at break	≥63%	≥63%		
Surface resistance	<10 $^{10}$ $\Omega$ /sq.	<10 $^{10}$ $\Omega$ /sq.		
Softening point	71 ±5 °C	71 ±5 °C		
Thickness	62 μm	62 μm		

#### **General information**

For the combination carrier/cover tape no electrostatic behaviour is observed (relative humidity  $\geq$ 30%). The products do not stick to the cover tape.

The technical and thermal properties of polycarbonate tapes are excellent, so there is no change in dimensions as a function of time. The peel off force is very stable as a function of time and temperature, and it is defined as 0.1 to 0.7 N at a peel-off speed of 120 mm/minute.

#### **Bulk packing**

For bulk case; see Fig.5 and Table 7.

# Surface-mount ceramic multilayer capacitors

### General data

#### Paper tape specifications

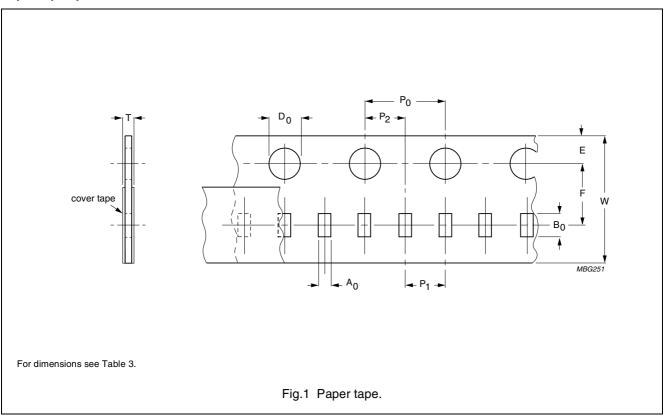


Table 3 Dimensions of paper tape for relevant product size; see Fig.1

			ĺ	PRODUCT	SIZE CODE				
SYMBOL	04	02	06	03	0805		1206		UNIT
	SIZE	TOL.	SIZE	TOL.	SIZE	TOL.	SIZE	TOL.	
A <sub>0</sub>	0.62	±0.05	1.10	±0.05	1.65	±0.05	2.0	±0.1	mm
B <sub>0</sub>	1.12	±0.05	1.90	±0.05	2.40	±0.05	3.5	±0.1	mm
W	8.0	±0.2	8.0	±0.2	8.0	±0.2	8.0	±0.2	mm
Е	1.75	±0.1	1.75	±0.1	1.75	±0.1	1.75	±0.1	mm
F	3.5	±0.05	3.5	±0.05	3.5	±0.05	3.5	±0.05	mm
D <sub>0</sub>	1.5	+0.1/-0	1.5	+0.1/-0	1.5	+0.1/-0	1.5	+0.1/-0	mm
P <sub>0</sub> ; note 1	4	±0.05	4	±0.05	4	±0.05	4	±0.05	mm
P <sub>1</sub>	2	±0.05	4	±0.1	4	±0.1	4	±0.1	mm
P <sub>2</sub>	2	±0.05	2	±0.05	2	±0.05	2	±0.05	mm
T <sub>max</sub>	0.6	±0.05	0.95	±0.05	0.95	±0.05	0.95	±0.05	mm

#### Note

1.  $P_0$  pitch tolerance over any 10 pitches is  $\pm 0.2$  mm.

### Surface-mount ceramic multilayer capacitors

#### General data

#### Blister tape specifications

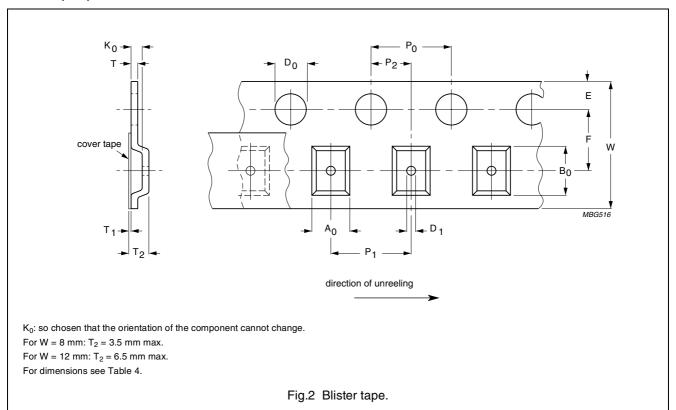


Table 4 Dimensions of blister tape for relevant product size code; see Fig.2

DIMENSION		PRODUCT SIZE CODE							
DIMENSION	0805	1206	1210	1812	2220	(mm)			
A <sub>0</sub> nominal clearance; note 1	0.20	0.30	0.30	0.40	0.40	-			
B <sub>0</sub> nominal clearance; note 1	0.20	0.30	0.30	0.40	0.40	-			
K <sub>0</sub> minimum clearance; note 1	0.05	0.05	0.05	0.05	0.05	-			
W	8.1	8.1	8.1	12.0	12.0	±0.2			
E	1.75	1.75	1.75	1.75	1.75	±0.1			
F	3.5	3.5	3.5	5.5	5.5	±0.05			
D <sub>0</sub>	1.5	1.5	1.5	1.5	1.5	+0.1/-0.0			
D <sub>1</sub>	≥1	≥1	≥1	1.5	1.5	+0.1/-0.0			
P <sub>0</sub> ; note 2	4	4	4	4	4	±0.1			
P <sub>1</sub>	4	4	4	8	8	±0.1			
P <sub>2</sub>	2	2	2	2	2	±0.05			

#### Notes

- 1. Typical capacitor displacement in pocket.
- 2.  $P_0$  pitch tolerance over any 10 pitches is  $\pm 0.2$  mm.

# Surface-mount ceramic multilayer capacitors

#### General data

#### **Reel specifications**

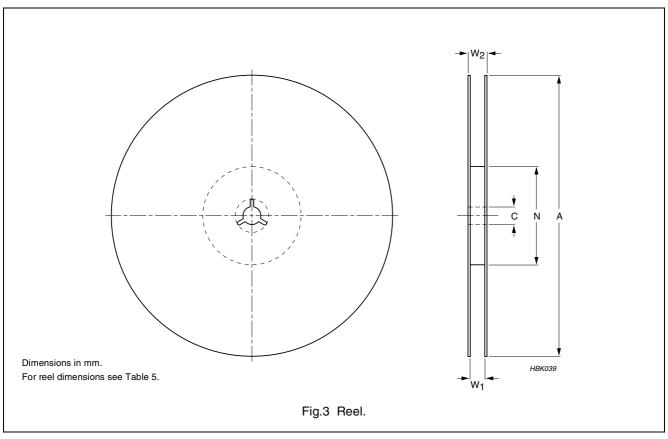


Table 5 Reel dimensions; see Fig.3

TAPE WIDTH (mm)	A (mm)	N (mm)	C (mm)	W <sub>1</sub> (mm)	W <sub>2</sub> MAX. (mm)
8	180	62 ±1.5	12.75 +0.15/-0	8.4 +1.5/-0.0	14.4
8	330	62 ±1.5	12.75 +0.15/-0	8.4 +1.5/-0.0	14.4
12	180	62 ±1.5	12.75 +0.15/-0	12.4 +2/-0.0	18.4

#### **Properties of reel**

Material: polystyrene

Surface resistance:  $<10^{10} \Omega/\text{sq}$ .

### Surface-mount ceramic multilayer capacitors

### General data

#### Leader/trailer tape specification

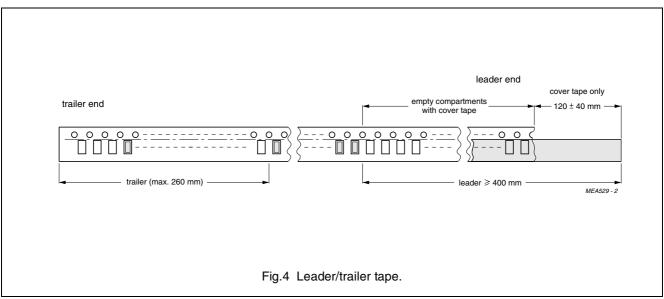


Table 6 Leader/trailer tape data

DESCRIPTION	VALUE
Minimum length of empty compartments at leader end	≥400 mm of which a minimum 240 mm of empty compartments are covered with cover tape and 120 ±40 mm cover tape only
Minimum length of empty compartments at trailer end	208 mm or 260 mm. If the length is 260 mm an extra product is placed at 208 mm to mark this position.

### Surface-mount ceramic multilayer capacitors

#### General data

#### **Bulk case specification**

In accordance with "IEC 60286-6".

Features and benefits:

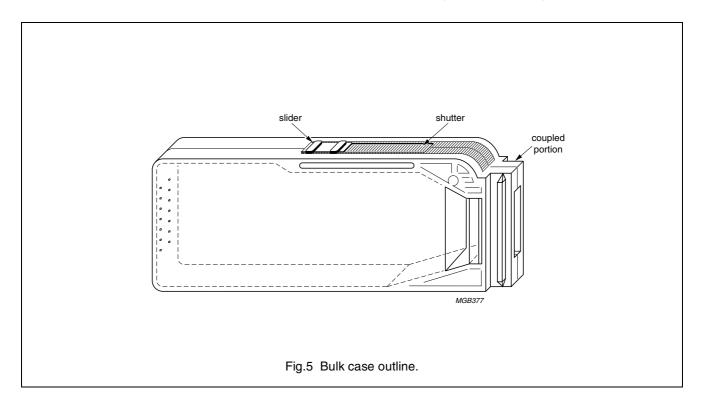
- Reduced costs
  - Storage
  - Transport
  - Machine handling
  - Packing
- Customized labelling (bar codes).

 Table 7
 Packing quantities for component size; see note 1 and Fig.5

SIZE CODE	DIMENS	DIMENSIONS OF CAPACITOR (mm)					
	L <sub>1</sub>	W	Т				
0402	1.0	0.5	0.5	50000			
0603	1.6	0.8	0.8	15000			
0805	2.0	1.25	0.6	10000			
0805	2.0	1.25	0.9	8000			
0805	2.0	1.25	1.25	5000			

#### Note

1. Refer to the selection charts in product data for specific values.



### Surface-mount ceramic multilayer capacitors

#### General data

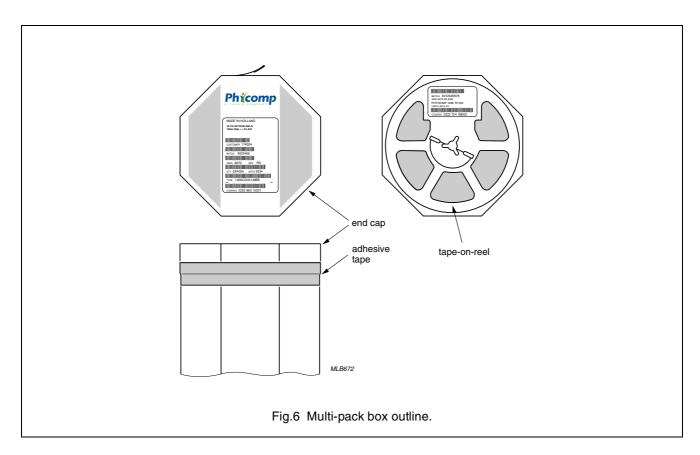
#### Multi-pack box specification

Features and benefits:

- Minimum recycling costs
- Maximum environmental friendliness
- Reduced handling time
- Economic usage of packing
- Customized labelling (bar codes).

Table 8 Number of reels per box; see Fig.6

REEL SIZE	TAPE SIZE	QUANTITY PER BOX			
(mm)	(mm)	MIN.	MAX.		
Ø180	8	5	25		
Ø180	12	5	10		
Ø330	8	5	15		

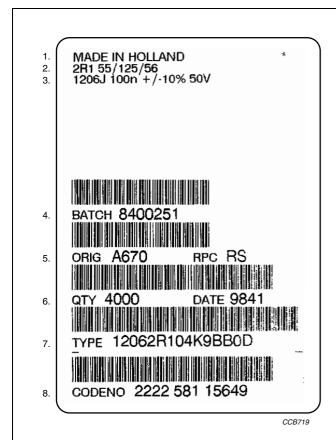


### Surface-mount ceramic multilayer capacitors

General data

#### **LABELLING**

Label examples are shown in Figs 7 and 8 (bar code according to EN 800 code 39).



#### LINE MARKING EXPLANATION

- 1. Country of origin
- 2. Material code and climatic category
- 3. Size, termination code, value, tolerance and rated voltage
- 4. Unique batch number
- Country of origin in code: A670 is Holland
- 6. Quantity and production period, year and week code
- 7. 15-digit Clear Text Code (CTC)
- 8. Catalogue number (12NC)

Fig.7 Packing label (example).



#### LINE MARKING EXPLANATION

- 1. Unique batch number
- 2. Quantity and date code
- Material code and climatic category
- 4. Size, termination code, value, tolerance and rated voltage
- 5. 15-digit Clear Text Code (CTC)
- 6. Catalogue number (12NC)

Fig.8 Reel label (example).

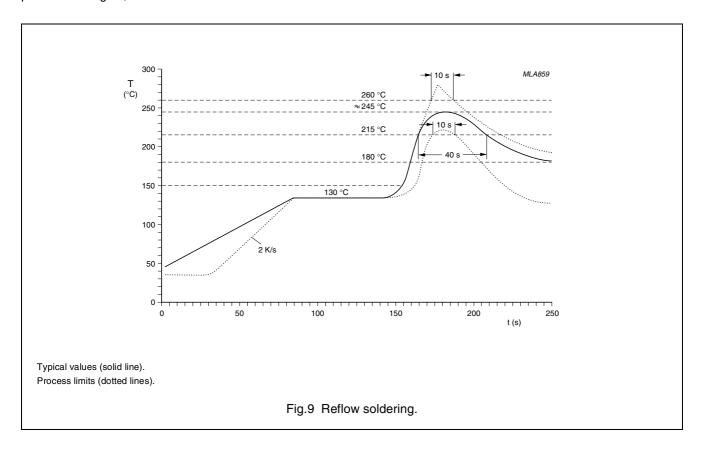
### Surface-mount ceramic multilayer capacitors

#### General data

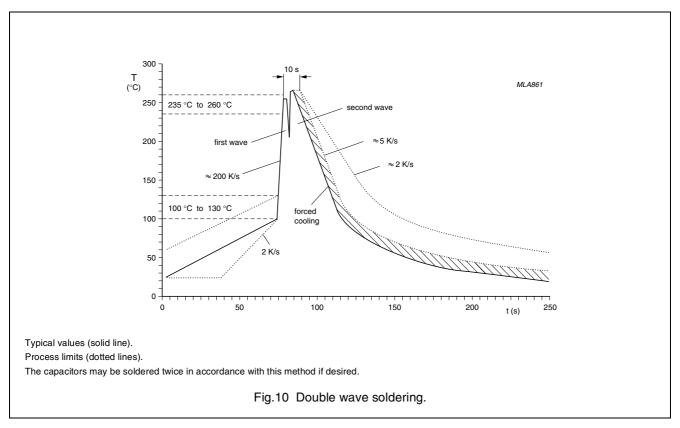
### METHOD OF MOUNTING AND FOOTPRINT DIMENSIONS

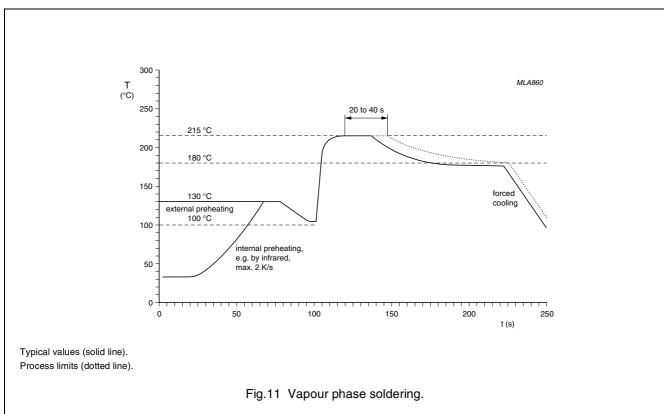
For normal use the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive in accordance with CECC 00802 classification A. For advised soldering profiles see Figs 9, 10 and 11.

An improper combination of soldering, substrate and chip size can lead to a damaging of the component. The risk increases with the chip size and with temperature fluctuations (>100 °C). Therefore, it is advised to use the smallest possible size and follow the dimensional recommendations given in Tables 9, 10 and 11 for reflow and wave soldering. More detailed information is available on request.



# Surface-mount ceramic multilayer capacitors





# Surface-mount ceramic multilayer capacitors

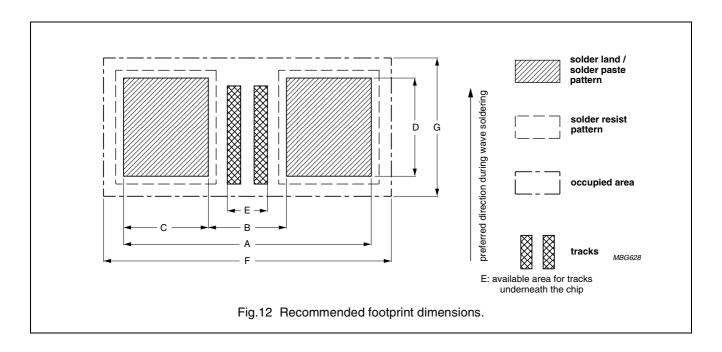


 Table 9
 Reflow soldering; for footprint dimensions see Fig.12

SIZE		F	OOTPRI	NT DIM (mm)	ENSION	NS	PROCESSING REMARKS	PLACEMENT ACCURACY	
CODE	Α	В	С	D	E	F	G		(mm)
0402	1.5	0.5	0.5	0.5	0.10	1.75	0.95		±0.15
0603	2.3	0.7	0.8	0.9	0.26	2.7	1.5		±0.15
0603	2.3	0.5	0.9	0.9	0.0	2.7	1.5	ID on bot plate a deleviron	±0.25
0805	2.8	0.9	0.95	1.4	0.45	3.2	2.1	IR or hot plate soldering	±0.25
1206	4.0	2.0	1.0	1.8	1.4	4.4	2.5		±0.25
1210	4.0	2.0	1.0	2.7	1.4	4.4	3.4		±0.25
1808	5.4	3.3	1.05	2.3	2.7	5.8	2.9		±0.25
1812	5.4	3.3	1.05	3.5	2.7	5.8	4.1	ceramic substrate only	±0.25
2220	6.6	4.5	1.05	5.3	3.9	7.0	5.9		±0.25

Table 10 Wave soldering (no dummy tracks allowed for ≥500 V); for footprint dimensions see Fig.12

SIZE	FOOTPRINT DIMENSIONS (mm)							PROPOSED NUMBER AND DIMENSIONS OF DUMMY	PLACEMENT ACCURACY	
CODE	A	В	С	D	E	F	G	TRACKS (mm)	(mm)	
0603	2.4	1.0	0.7	0.8	0.2	3.0	1.9	1 × (0.2 × 0.8)	±0.10	
0603	2.7	0.9	0.9	0.8	0.0	3.2	2.1	$1\times(0.3\times0.8)$	±0.25	
0805	3.2	1.4	0.9	1.3	0.36	4.1	2.5	1 × (0.3 × 1.3)	±0.15	
0805	3.4	1.3	1.05	1.3	0.2	4.3	2.7	1 × (0.2 × 1.3)	±0.25	
1206	4.8	2.3	1.25	1.7	1.25	5.9	3.2	3 × (0.25 × 1.7)	±0.25	
1210	5.3	2.3	1.5	2.6	1.25	6.3	4.2	$3 \times (0.25 \times 2.6)$	±0.25	

# Surface-mount ceramic multilayer capacitors

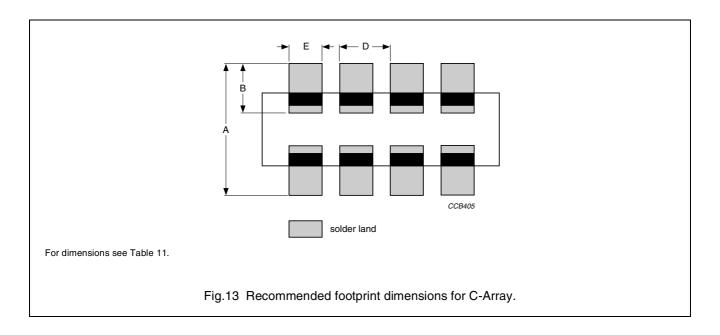


Table 11 C-Array footprint dimensions; see Fig.13

CASE SIZE	FOOTPRINT DIMENSIONS (mm)							
SIZE	Α	В	С	D	E			
0612 (4 × 0603)	2.54 ±0.15	0.89 ±0.10	0.76 ±0.10	0.80 ±0.10	0.45 ±0.10			

# Surface-mount ceramic multilayer capacitors

#### General data

#### **TEST CONDITIONS IN STATIC SOLDER BATH**

PARAMETER	DESCRIPTION		
Solderability			
95% covered with smooth and bright solder coating	CECC requirement: 235 ±5 °C for 2 ±0.5 s		
	IEC requirement: 215 ±3 °C for 3 ±0.3 s		
Resistance to leaching			
10% of the metallization of the edges of the head face may be missing (inner electrodes are not visible)	260 ±5 °C for 30 ±1 s		

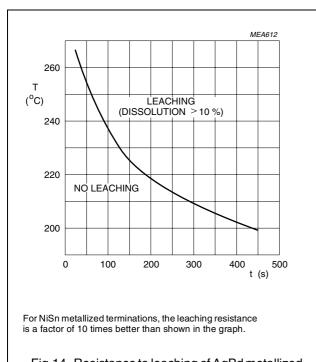


Fig.14 Resistance to leaching of AgPd metallized terminations (in static solder bath) at various temperatures.

# Surface-mount ceramic multilayer capacitors

General data

#### **TESTS AND REQUIREMENTS**

Table 12 Test procedures and requirements

IEC 60384-10/ 60068-2 TEST METHOD		TEST	PROCEDURE	REQUIREMENTS	
4.4		mounting	the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive	no visible damage	
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification	
4.6.1		capacitance	class 1: C ≤ 1000 pF, f = 1 MHz; C > 1000 pF, f = 1 kHz; NP0: measuring voltage 1 V at 20 °C	within specified tolerance	
			class 2: for all capacitors f = 1 kHz; X7R: measuring voltage 1 V at 20 °C Y5V/Z5U: measuring voltage 1 V at 25 °C		
4.6.2		tan δ	class 1: $C \le 1000 \text{ pF, f} = 1 \text{ MHz;}$ C > 1000  pF, f = 1  kHz; NP0: measuring voltage 1 V at 20 °C	in accordance with specification	
			class 2: for all capacitors f = 1 kHz; X7R: measuring voltage 1 V at 20 °C Y5V/Z5U: measuring voltage 1 V at 25 °C		
4.6.3		insulation resistance	at U <sub>R</sub> (DC) for 1 minute	in accordance with specification	
4.6.4		voltage proof	$\begin{array}{l} U_R \leq 100 \text{ V:} \\ 2.5 \times U_R \text{ for 1 minute;} \\ U_R > 100 \text{ V:} \\ 1.5 \times U_R + 100 \text{ for 1 minute} \end{array}$	no breakdown or flashover	
4.7.1		temperature coefficient	class 1: between minimum and maximum temperature	in accordance with specification	
4.7.2	temperature characteristic		class 2: between minimum and maximum temperature	in accordance with specification	

# Surface-mount ceramic multilayer capacitors

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with CECC 32 100, paragraph 4.4	no visible damage
			conditions: bending 1 mm at a rate of 1 mm/s, radius jig. 340 mm	$\Delta$ C/C: class 1: within ±10% class 2, X7R: within ±10% class 2, Y5V: within ±30%
4.10	Tb	resistance to soldering heat	260 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery
				$\Delta$ C/C: class 1: within ±0.5% or 0.5 pF whichever is greater class 2, X7R: >-5% and ≤10% class 2, Y5V: >-10% and ≤20%
		resistance to leaching	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%
4.11	Та	solderability	zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere; unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C	the terminations shall be well tinned

# Surface-mount ceramic multilayer capacitors

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.12	Na	rapid change of temperature	preconditioning, class 2 only: NP0/X7R: -55 to +125 °C; 5 cycles Y5V: -25 to +85 °C; 5 cycles	no visible damage after 24 hours recovery $\Delta C/C$ : class 1: within $\pm 1\%$ or 1 pF class 2, X7R: within $\pm 15\%$ class 2, Y5V: within $\pm 20\%$
4.14	Са	damp heat	preconditioning, class 2 only: 56 days at 40 °C; 90 to 95% RH; U <sub>R</sub> applied (max. 500 V)	no visual damage after recovery class 1: 1 to 2 hours class 2: 24 hours ΔC/C: class 1: within ±2% or 1 pF, whichever is greater
			class 2, X7R: within ±15%, ±20% class 2, Y5V: within ±30%, +30/–40% (according to Phycomp specification) tan δ:	
		class 1: ≤2 × specified value class 2: X7R: ≤7% class 2: Y5V: ≤12.5%, 15% (according to Phycomp specification)		
				$\begin{aligned} &R_{\text{ins}}\text{:}\\ &\text{class 1:}\\ &2500 \text{ M}\Omega \text{ or } R_i C_R \geq 25 \text{ s,}\\ &\text{whichever is less}\\ &\text{class 2:}\\ &1000 \text{ M}\Omega \text{ or } R_i C_R \geq 25 \text{ s,}\\ &\text{whichever is less} \end{aligned}$

# Surface-mount ceramic multilayer capacitors

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.15		endurance	preconditioning, class 2 only: 1000 hours at upper category temperature at: $2 \times U_R$ for $U_R \le 50$ V; $1.5 \times U_R$ for other rated voltages	no visible damage after 24 hours recovery: $\Delta C/C:$ class 1: within $\pm 2\%$ or 1 pF, whichever is greater class 2, X7R: within $\pm 20\%$ class 2, Y5V: within $\pm 30\%$ , $+30/-40\%$ (according to Phycomp specification) tan $\delta$ : class 1: $\leq 2 \times$ specified value class 2: X7R: $\leq 7\%$ class 2: Y5V: $\leq 12.5\%$ , 15% (according to Phycomp specification) $R_{ins}:$ class 1: $4000~M\Omega$ or $R_iC_R \geq 40~s$ , whichever is less class 2: $2~000~M\Omega$ or $R_iC_R \geq 50~s$ , whichever is less

# Surface-mount ceramic multilayer capacitors

### General data

#### **REVISION HISTORY**

Revision	Date	Change Notification	Description
Rev.6	2001 May 30	_	- Converted to Phycomp brand