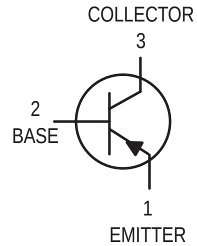
General Purpose Transistors

PNP Silicon Annular Hermetic Transistors

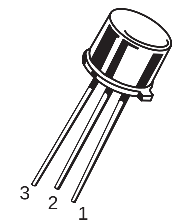
Designed for high–speed switching circuits, DC to VHF amplifier applications and complementary circuitry.

- High DC Current Gain Specified — 0.1 to 500 mAdc
- High Current–Gain — Bandwidth Product — f_T = 200 MHz (Min) @ I_C = 50 mAdc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.4 Vdc (Max) @ I_C = 150 mAdc
- 2N2904A thru 2N2907, A Complement to NPN 2N2219, A, 2N2222, A

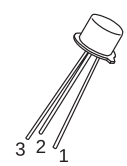


2N2904A* thru 2N2907,A*

*2N2904A, 2N2905A and 2N2907A are Motorola Preferred Devices



**2N2904A/2N2905,A
CASE 79–04, STYLE 1
TO–39 (TO–205AD)**



**2N2906A/2N2907,A
CASE 22–03, STYLE 1
TO–18 (TO–206AA)**

MAXIMUM RATINGS

Rating	Symbol	Non–A Suffix	A–Suffix	Unit
Collector–Emitter Voltage	V_{CEO}	–40	–60	Vdc
Collector–Base Voltage	V_{CBO}	–60		Vdc
Emitter–Base Voltage	V_{EBO}	–5.0		Vdc
Collector Current — Continuous	I_C	–600		mAdc
		2N2904A 2N2905,A	**2N2906A 2N2907,A**	
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	600 3.43	400 2.28	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	1.2 6.85	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

HERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		2N2904A 2N2905,A	**2N2906A 2N2907,A**	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	292	438	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	58	146	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage(1) (I_C = –10 mAdc, I_B = 0)	Non–A Suffix A–Suffix	$V_{(BR)CEO}$	–40 –60	— —	— —	Vdc
Collector–Base Breakdown Voltage (I_C = –10 μAdc, I_E = 0)		$V_{(BR)CBO}$	–60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = –10 μAdc, I_C = 0)		$V_{(BR)EBO}$	–5.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = –30 Vdc, V_{EB} = –0.5 Vdc)		I_{CEX}	—	—	–50	nAdc
Collector Cutoff Current (V_{CB} = –50 Vdc, I_E = 0) (V_{CB} = –50 Vdc, I_E = 0, T_A = 150°C)	 Non–A Suffix A–Suffix Non–A Suffix A–Suffix	I_{CBO}	 — — — —	 — — — —	 –0.02 –0.01 –20 –10	μAdc
Base Current (V_{CE} = –30 Vdc, V_{EB} = –0.5 Vdc)		I_B	—	—	–50	nAdc

1. Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

(Replaces 2N2904/D)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = –0.1 mAdc, V_{CE} = –10 Vdc)	2N2905, 2N2907		35	—	—	
	2N2904A, 2N2906A		40	—	—	
	2N2905A, 2N2907A		75	—	—	
(I_C = –1.0 mAdc, V_{CE} = –10 Vdc)	2N2905, 2N2907		25	—	—	
	2N2904A, 2N2906A		40	—	—	
	2N2905A, 2N2907A		100	—	—	
(I_C = –10 mAdc, V_{CE} = –10 Vdc)	2N2905, 2N2907		75	—	—	
	2N2904A, 2N2906A		40	—	—	
	2N2905A, 2N2907A		100	—	—	
(I_C = –150 mAdc, V_{CE} = –10 Vdc)(1)	2N2904A, 2N2906A		40	—	120	
	2N2905,A, 2N2907,A		100	—	300	
(I_C = –500 mAdc, V_{CE} = –10 Vdc)(1)	2N2905, 2N2907		30	—	—	
	2N2904A, 2N2906A		40	—	—	
	2N2905A, 2N2907A		50	—	—	
Collector–Emitter Saturation Voltage(1)		$V_{CE(sat)}$				Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)			—	—	–0.4	
(I_C = –500 mAdc, I_B = –50 mAdc)			—	—	–1.6	
Base–Emitter Saturation Voltage(1)		$V_{BE(sat)}$				Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)			—	—	–1.3	
(I_C = –500 mAdc, I_B = –50 mAdc)			—	—	–2.6	
YNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product(2) (I_C = –50 mAdc, V_{CE} = –20 Vdc, f = 100 MHz)		f_T	200	—	—	MHz
Output Capacitance (V_{CB} = –10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	—	8.0	pF
Input Capacitance (V_{EB} = –2.0 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	—	—	30	pF
WITCHING CHARACTERISTICS						
Turn–On Time	(V_{CC} = –30 Vdc, I_C = –150 mAdc, I_{B1} = –15 mAdc) (Figure 15a)	t_{on}	—	26	45	ns
Delay Time		t_d	—	6.0	10	
Rise Time		t_r	—	20	40	
Turn–Off Time	(V_{CC} = –6.0 Vdc, I_C = –150 mAdc, I_{B1} = I_{B2} –15 mAdc) (Figure 15b)	t_{off}	—	70	100	ns
Storage Time		t_s	—	50	80	
Fall Time		t_f	—	20	30	

1. Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

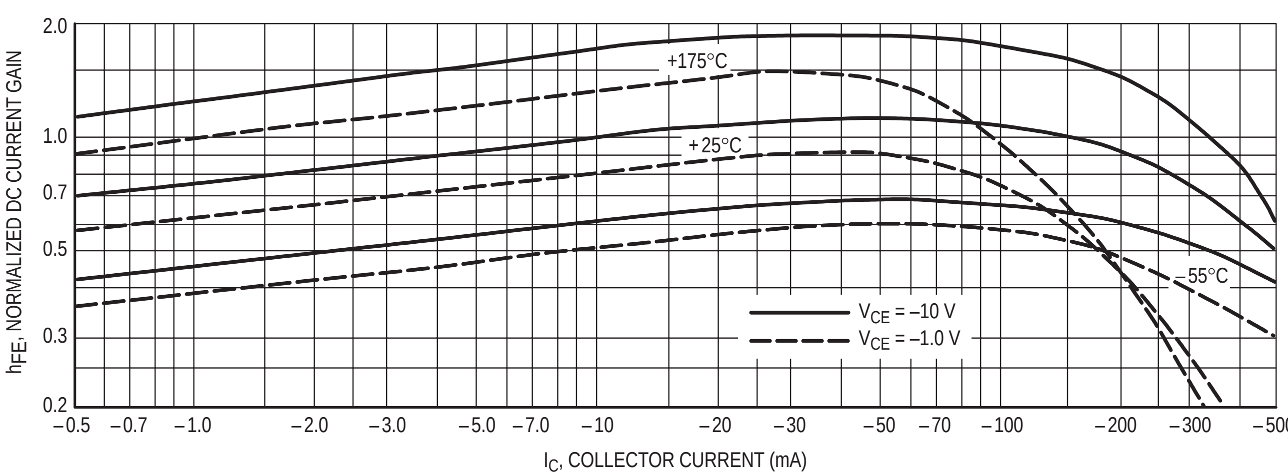
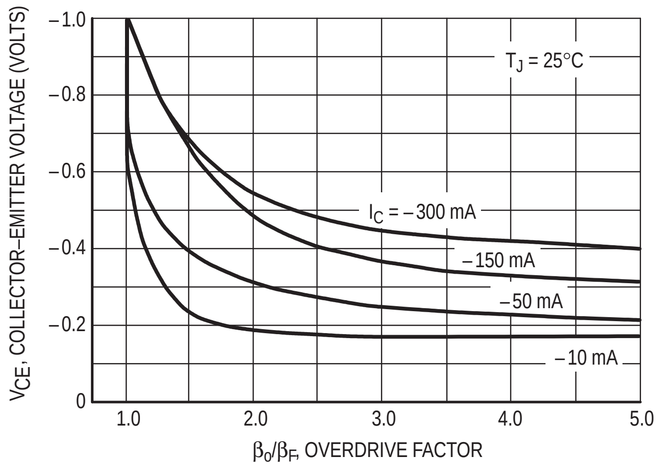


Figure 1. Normalized DC Current Gain



This graph shows the effect of base current on collector current. β_o (current gain at the edge of saturation) is the current gain of the transistor at 1 volt, and β_F (forced gain) is the ratio of I_C/I_{BF} in a circuit.

EXAMPLE: For type 2N2905, estimate a base current (I_{BF}) to ensure saturation at a temperature of 25°C and a collector current of 150 mA.

Observe that at I_C = 150 mA an overdrive factor of at least 3 is required to drive the transistor well into the saturation region. From Figure 1, it is seen that h_{FE} @ 1 volt is approximately 0.6 of h_{FE} @ 10 volts. Using the guaranteed minimum of 100 @ 150 mA and 10 V, β_o = 60 and substituting values in the overdrive equation, we find:

$$\frac{\beta_o}{\beta_F} = \frac{h_{FE} \text{ @ } 1.0 \text{ V}}{I_C/I_{BF}} \qquad 3 = \frac{60}{150/I_{BF}} \qquad I_{BF} \approx 7.5 \text{ mA}$$

Figure 2. Normalized Collector Saturation Region

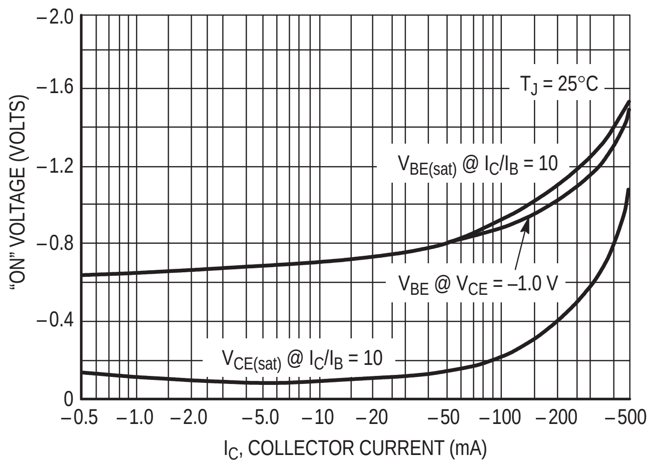


Figure 3. "On" Voltages

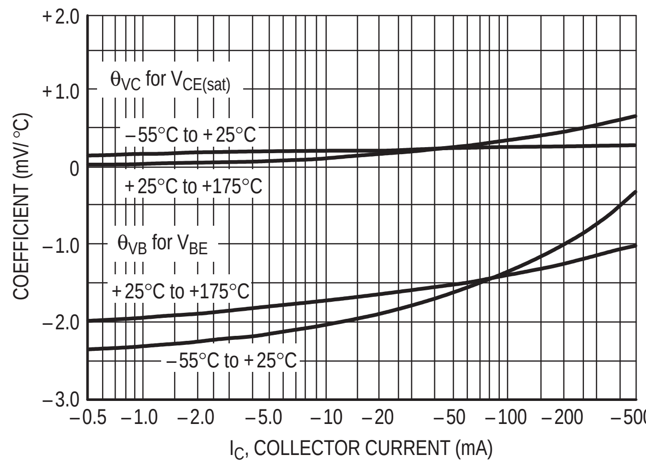


Figure 4. Temperature Coefficients

SMALL–SIGNAL CHARACTERISTICS

NOISE FIGURE

V_{CE} = 10 V, T_A = 25°C

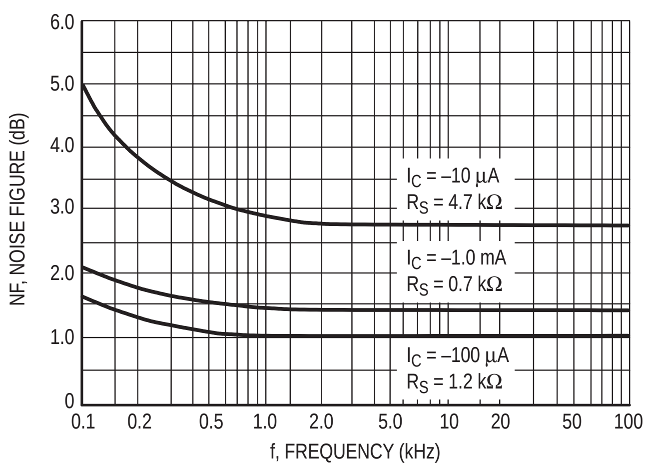


Figure 5. Frequency Effects

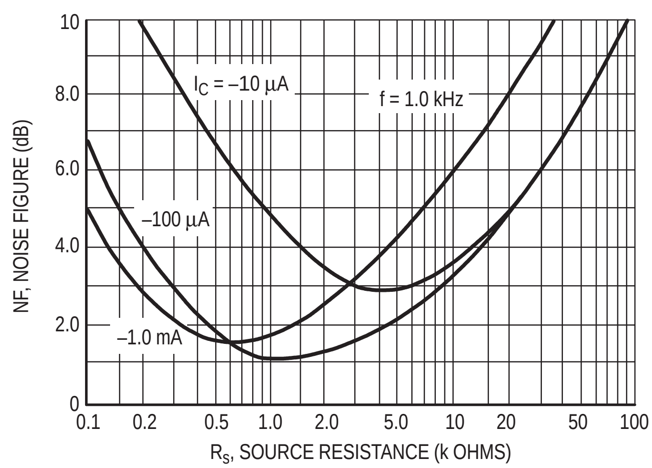


Figure 6. Source Resistance Effects

h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high–gain and a low–gain unit were selected and the same units were used to develop the correspondingly numbered curves on each graph.

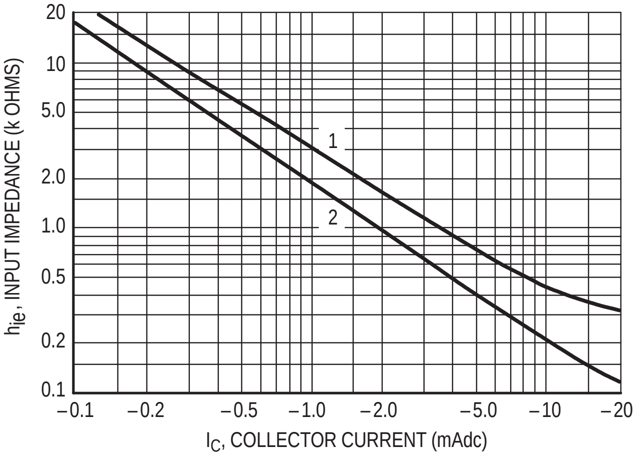


Figure 7. Input Impedance

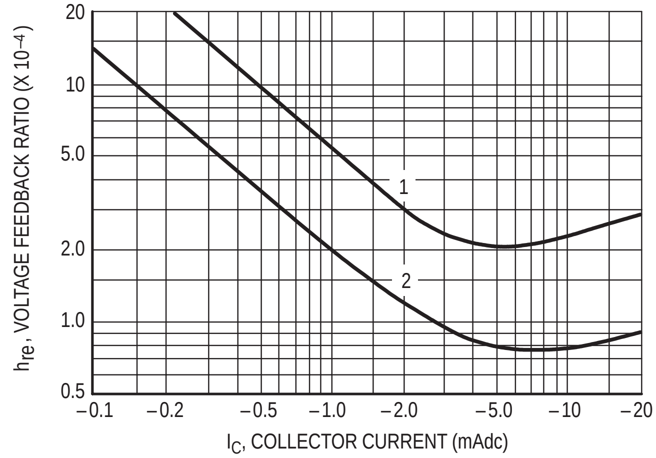


Figure 8. Voltage Feedback Ratio

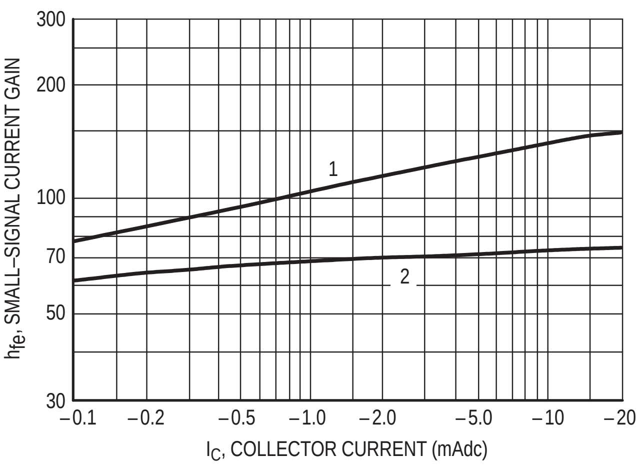


Figure 9. Current Gain

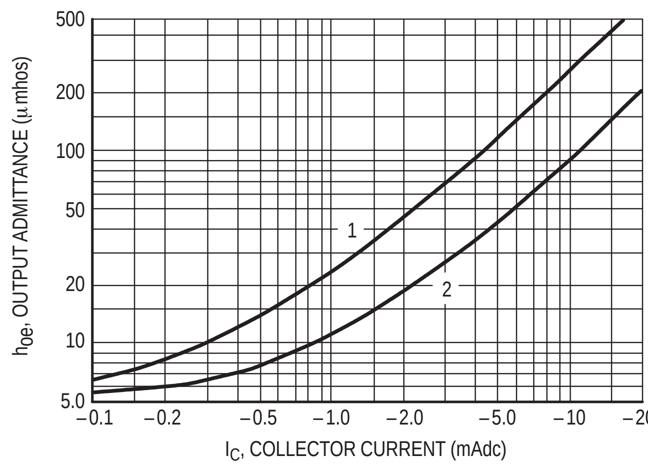


Figure 10. Output Admittance

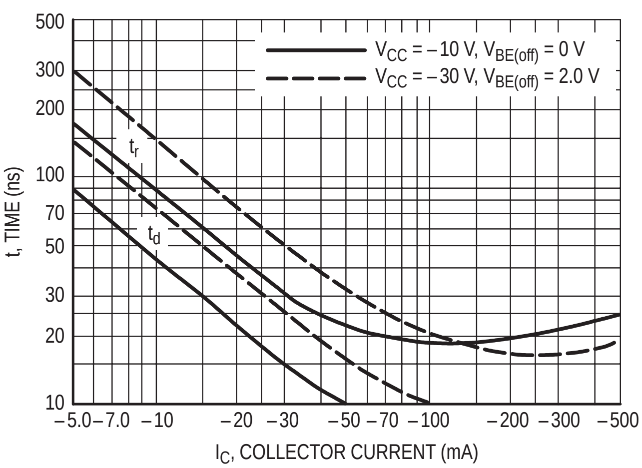


Figure 11. Turn–On Time

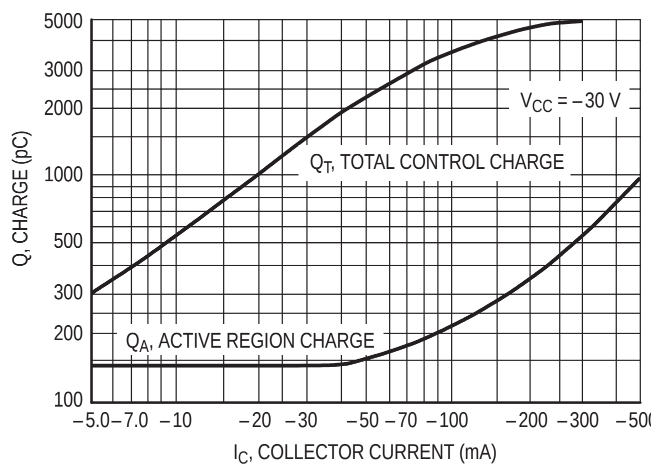


Figure 12. Charge Data

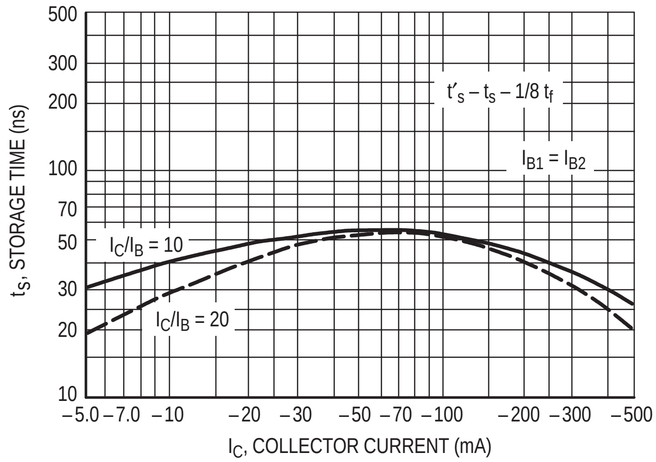


Figure 13. Storage Time

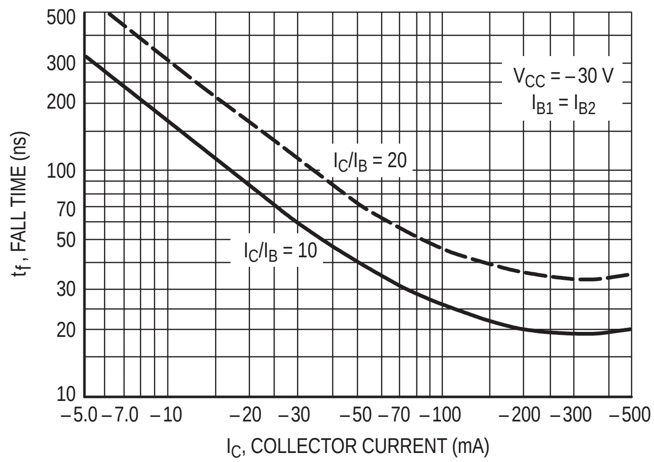


Figure 14. Fall Time

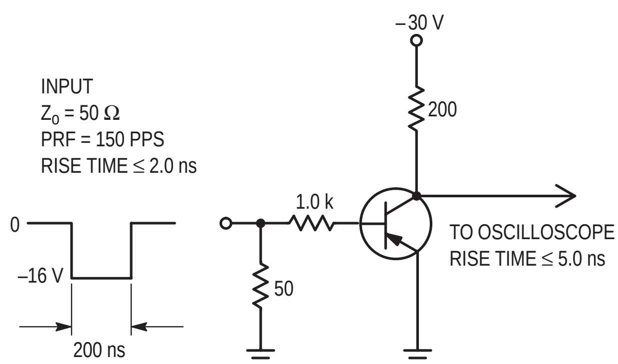


Figure 15a. Delay and Rise Time Test Circuit

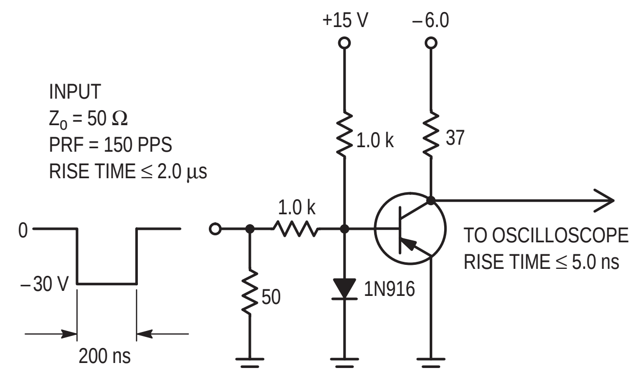


Figure 15b. Storage and Fall Time Test Circuit

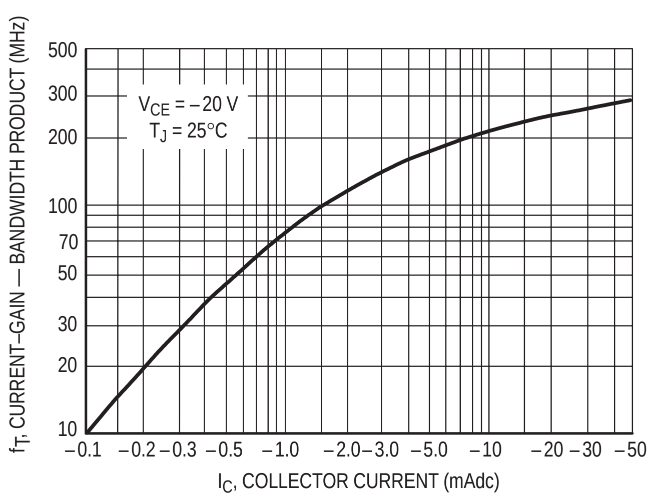


Figure 16. Current–Gain — Bandwidth Product

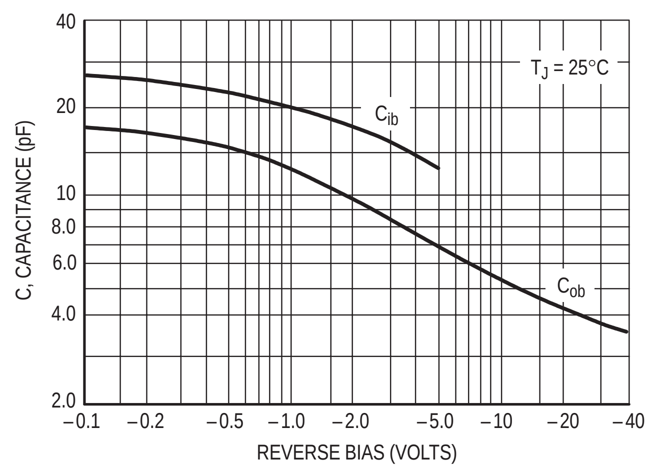
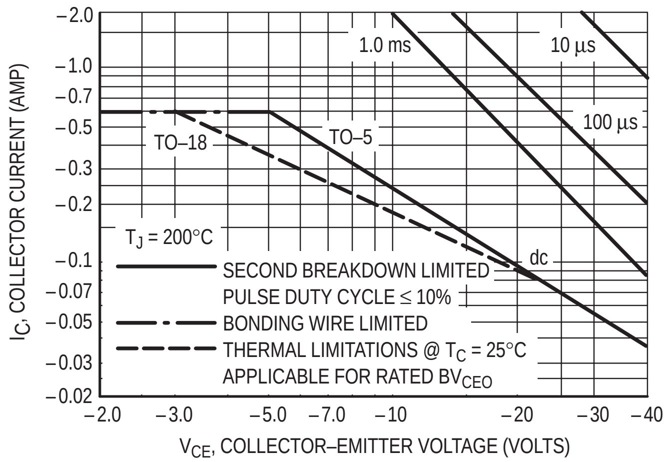


Figure 17. Capacitances



This graph shows the maximum I_C–V_{CE} limits of the device both from the standpoint of thermal dissipation (at 25°C case temperature), and secondary breakdown. For case temperatures other than 25°C, the thermal dissipation curve must be modified in accordance with the derating factor in the Maximum Ratings table.

To avoid possible device failure, the collector load line must fall below the limits indicated by the applicable curve. Thus, for certain operating conditions the device is thermally limited, and for others it is limited by secondary breakdown.

For pulse applications, the maximum I_C–V_{CE} product indicated by the dc thermal limits can be exceeded. Pulse thermal limits may be calculated by using the transient thermal resistance curve of Figure 19.

Figure 18. Active Region Safe Operating Areas

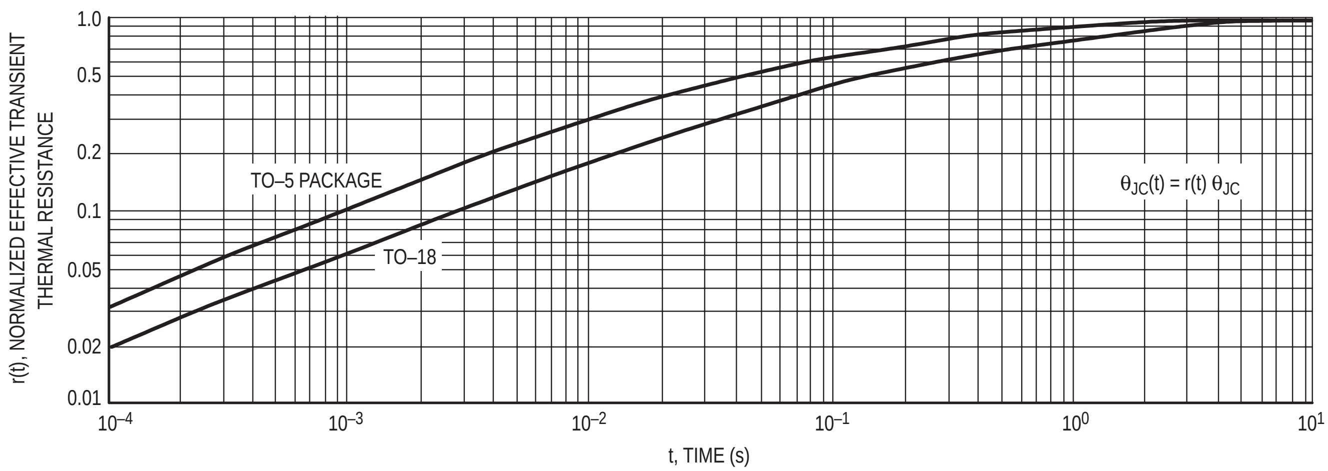
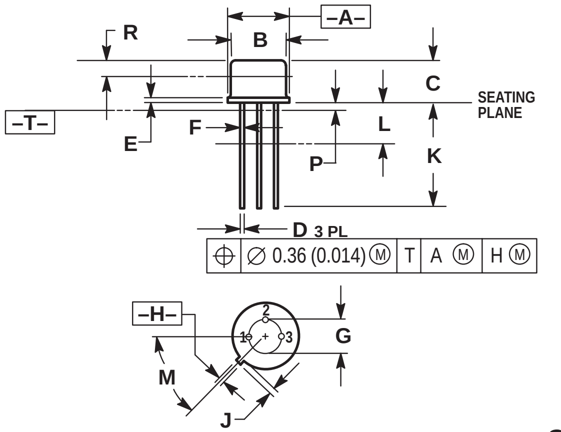


Figure 19. Thermal Resistance

PACKAGE DIMENSIONS

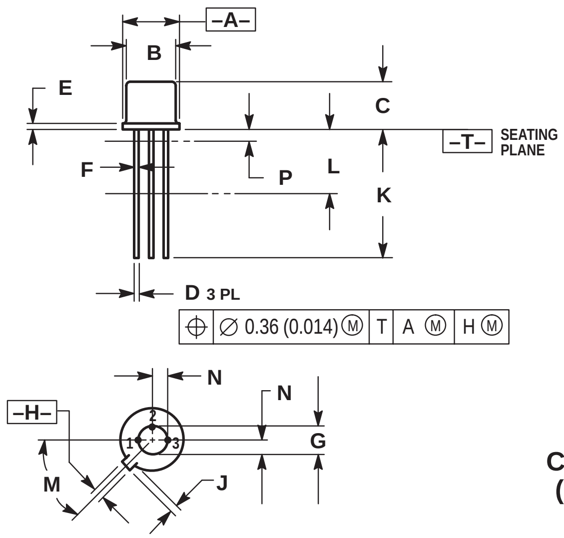


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.335	0.370	8.51	9.39
B	0.305	0.335	7.75	8.50
C	0.240	0.260	6.10	6.60
D	0.016	0.021	0.41	0.53
E	0.009	0.041	0.23	1.04
F	0.016	0.019	0.41	0.48
G	0.200 BSC		5.08 BSC	
H	0.028	0.034	0.72	0.86
J	0.029	0.045	0.74	1.14
K	0.500	0.750	12.70	19.05
L	0.250	—	6.35	—
M	45°BSC		45°BSC	
P	—	0.050	—	1.27
R	0.100	—	2.54	—

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 079–04
(TO–205AD)
ISSUE N



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.
5. DIMENSION E INCLUDES THE TAB THICKNESS. (TAB THICKNESS IS 0.51(0.002) MAXIMUM).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.209	0.230	5.31	5.84
B	0.178	0.195	4.52	4.95
C	0.170	0.210	4.32	5.33
D	0.016	0.021	0.406	0.533
E	—	0.030	—	0.762
F	0.016	0.019	0.406	0.483
G	0.100 BSC		2.54 BSC	
H	0.036	0.046	0.914	1.17
J	0.028	0.048	0.711	1.22
K	0.500	—	12.70	—
L	0.250	—	6.35	—
M	45°BSC		45°BSC	
N	0.050 BSC		1.27 BSC	
P	—	0.050	—	1.27

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 022–03
(TO–206AA)
ISSUE N

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