

The UPB569 is a low voltage dual modulus prescaler for operation frequency up to 500 MHz. High performance PLL frequency synthesizer systems can be realized using the UPB569.

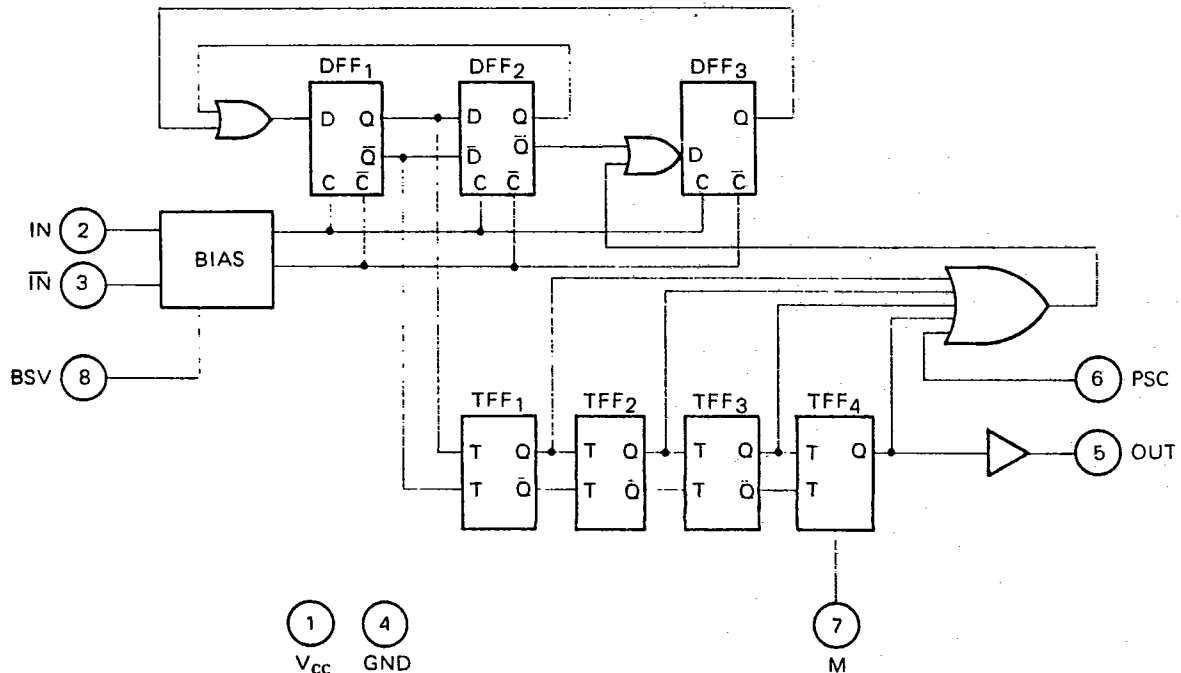
FEATURES

- Low supply voltage : $V_{CC} = 2.9 \text{ V MIN.}$
- Low supply current : $I_{CC} = 5.6 \text{ mA TYP. (} V_{CC} = 3.3 \text{ V)}$
- Pulse swallowing operation : $\div 32/\div 33, \div 64/\div 65$
- High frequency operation : f_{in} : 100 to 550 MHz ($V_{in} = 160 \text{ mV}_{p-p}$)
- Operation is guaranteed : $-30 \text{ to } +85 \text{ }^\circ\text{C}$

ORDERING INFORMATION

Order Code	Package
μ PB569C	8 pin plastic DIP (300 mil)
μ PB569G	8 pin plastic SOP (225 mil)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = 25\text{ }^\circ\text{C}$)

Supply Voltage	V_{cc}	-0.5 to +6.0	V
Input Voltage	V_{I1}	-0.5 to $V_{cc} + 0.5$	V
Input Voltage	V_{I2}^*	-0.5 to V_{cc}	V
Output Current	I_o	-10	mA
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

*BSV pin

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{cc}	2.9	3.3	5.5	V	
Ambient Temperature	T_a	-35	25	85	$^\circ\text{C}$	
Output Load Capacitance	C_L			10	pF	

ELECTRIC CHARACTERISTICS ($V_{cc} = 2.9$ to 5.5 V , $T_a = -35$ to $85\text{ }^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Current	I_{cc1}		5.6	7.5	mA	$V_{cc} = 3.3\text{ V}$
Supply Current	I_{cc2}		7.0	10	mA	$V_{cc} = 5.5\text{ V}$
Output Voltage	V_o	0.8		1.4	Vp-p	OUT pin, $C_L = 10\text{ pF}$
Input Voltage	V_{in}	160		630	mVp-p	IN pin ($f_{in} = 100$ to 550 MHz)
High Level Input Voltage	V_{IH1}	$V_{cc} - 0.4$			V	PSC, M pin
Low Level Input Voltage	V_{IL1}			$0.4 V_{cc}$	V	PSC, M pin
High Level Input Current	I_{IH}			35	μA	PSC, M pin
Low Level Input Current	I_{IL}	-150			μA	PSC, M pin
High Level Input Voltage	V_{IH2}	2.7			V	BSV pin
Low Level Input Voltage	V_{IL2}	0		0.4	V	BSV pin
Supply Current	I_{cc3}			10	μA	BSV = Low
Operating Frequency	f_{in}	100		550	MHz	IN pin ($V_{in} = 160\text{ mVp-p}$)
Set Up Time	t_s			20	ns	PSC \rightarrow OUT

DIVISION RATIO CONTROL

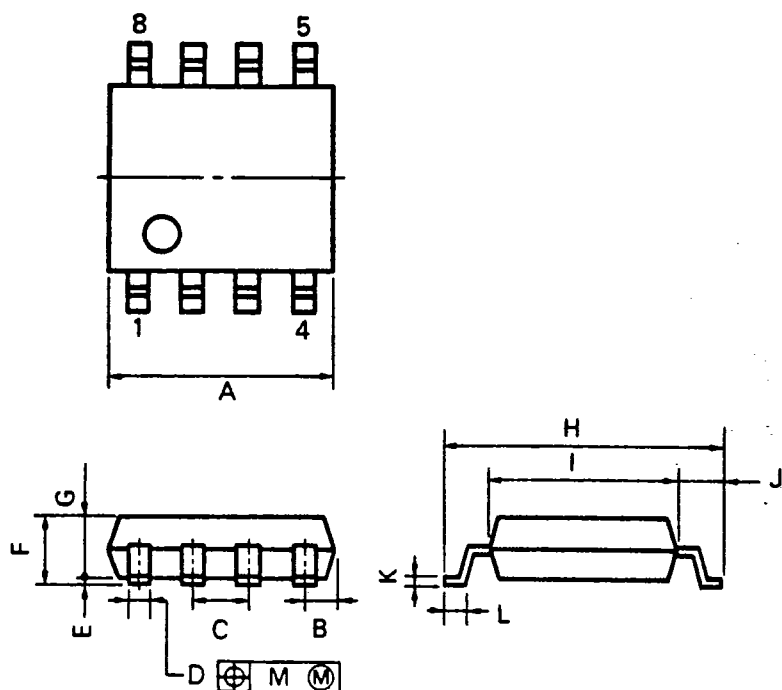
M	PSC	DIVISION RATIO
L	H	$\div 64$
L	L	$\div 65$
H	H	$\div 32$
H	L	$\div 33$

H: $V_{cc} - 0.4$ to V_{cc}

L: 0 to $0.4 V_{cc}$

PACKAGE DIMENSION

8 PIN PLASTIC SOP (225 mil)

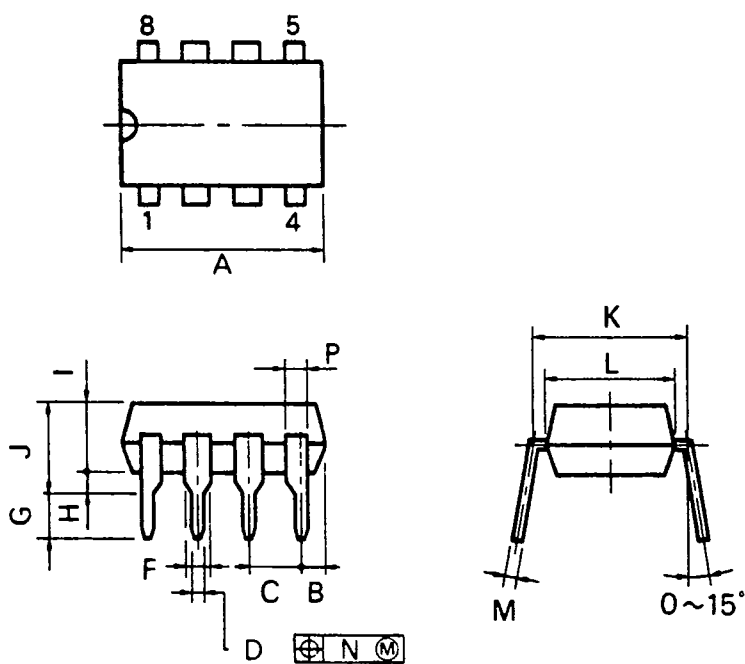


ITEM	MILLIMETERS	INCHES
A	5.70 MAX.	0.225 MAX.
B	0.94 MAX.	0.037 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 $^{+0.05}$	0.016 $^{+0.002}$
E	0.1 $^{+0.1}$	0.004 $^{+0.004}$
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5 $^{+0.3}$	0.256 $^{+0.012}$
I	4.4	0.173
J	1.1	0.043
K	0.15 $^{+0.10}$	0.006 $^{+0.002}$
L	0.6 $^{+0.2}$	0.024 $^{+0.008}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

8 PIN PLASTIC DIP (300 mil)

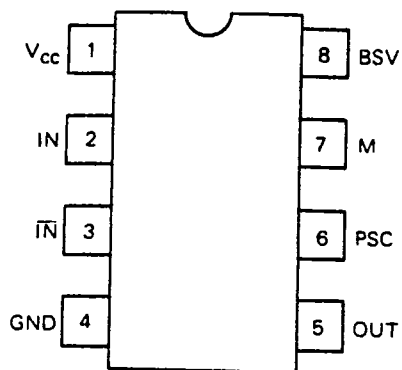


ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 $^{+0.10}$	0.020 $^{+0.004}$
F	1.4 MIN.	0.055 MIN.
G	3.2 $^{+0.3}$	0.126 $^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 $^{+0.10}$	0.010 $^{+0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

CONNECTION DIAGRAM (Top View)

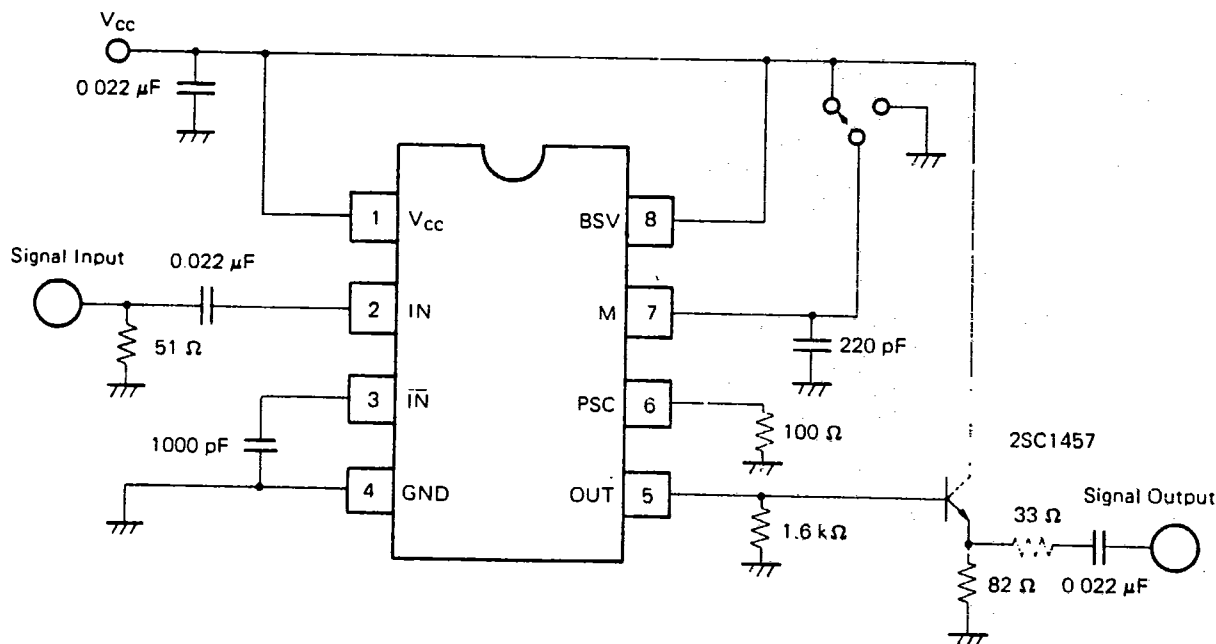


PIN No.	SYMBOL	FUNCTION
1	V _{cc}	Power Supply
2	IN	Signal Input (Positive Logic)
3	$\overline{\text{IN}}$	Signal Input (Negative Logic)
4	GND	GND
5	OUT	Signal Output
6	PSC	Pulse Swallow Control
7	M	Division Ratio Control
8	BSV	Battery Save

Note: Battery Saving Mode

In case BSV input pin becomes "Low" level, battery saving mode starts. In battery saving mode, μPB569 stops functioning and supply current becomes less than 10 μA .

TEST CIRCUIT



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