

SDA 2211 Pre-scaler 1:64 for 1.3 GHz with Low Current Consumption

Preliminary data

The IC has been designed for application in TV receivers using the frequency control of the frequency synthesis rough copy concept. It includes a pre-amplifier and an ECL pre-scaler with a 1:64 scaling rate and symmetrical ECL push-pull outputs. The operating range of the IC extends to an input frequency of 1.3 GHz.

- Minimal current consumption
- High input sensitivity

Maximum ratings

| | | | |
|-----------------------------------|-------------|-----------|----------|
| Supply voltage | V_S | -0.3 to 6 | V |
| Input voltage | $V_{i2,3}$ | 2.5 | V_{PP} |
| Output voltage | $V_{q6,7}$ | V_S | V |
| Output current | $-I_{q6,7}$ | 10 | mA |
| Junction temperature | T_j | 125 | °C |
| Storage temperature range | T_{stg} | 40 to 125 | °C |
| Thermal resistance: System-air | R_{thSA} | 115 | K/W |

Range of operation

| | | | |
|---------------------------|-----------|------------|-----|
| Supply voltage | V_S | 4.5 to 5.5 | V |
| Input frequency | f | 70 to 1300 | MHz |
| Ambient temperature range | T_{amb} | 0 to 70 | °C |

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Characteristics ($V_S = 4.5 - 5.5$ V; $T_{amb} = 0 - 70^\circ\text{C}$)

| | min | typ | max | |
|---|-------------|-----|-----|------------|
| Current consumption inputs blocked, outputs free | | 23 | 29 | mA |
| Output voltage shift (at each output) $C_L \leq 15$ pF $C_L = 60$ pF | 0.5 0.35 | 1 | 1.2 | dBm dBm |
| Input level ("Input sensitivity") | | | | |
| 70 MHz | -26 | | 3 | dBm |
| 80 MHz | -27 | | 3 | dBm |
| 120 MHz | -30 | | 3 | dBm |
| 250 MHz | -32 | | 3 | dBm |
| 600 MHz | -27 | | 3 | dBm |
| 1000 MHz | -27 | | 3 | dBm |
| 1100 MHz | -27 | | 3 | dBm |
| 1200 MHz | -21 | | 3 | dBm |
| 1300 MHz | -15 | | 3 | dBm |

Circuit description

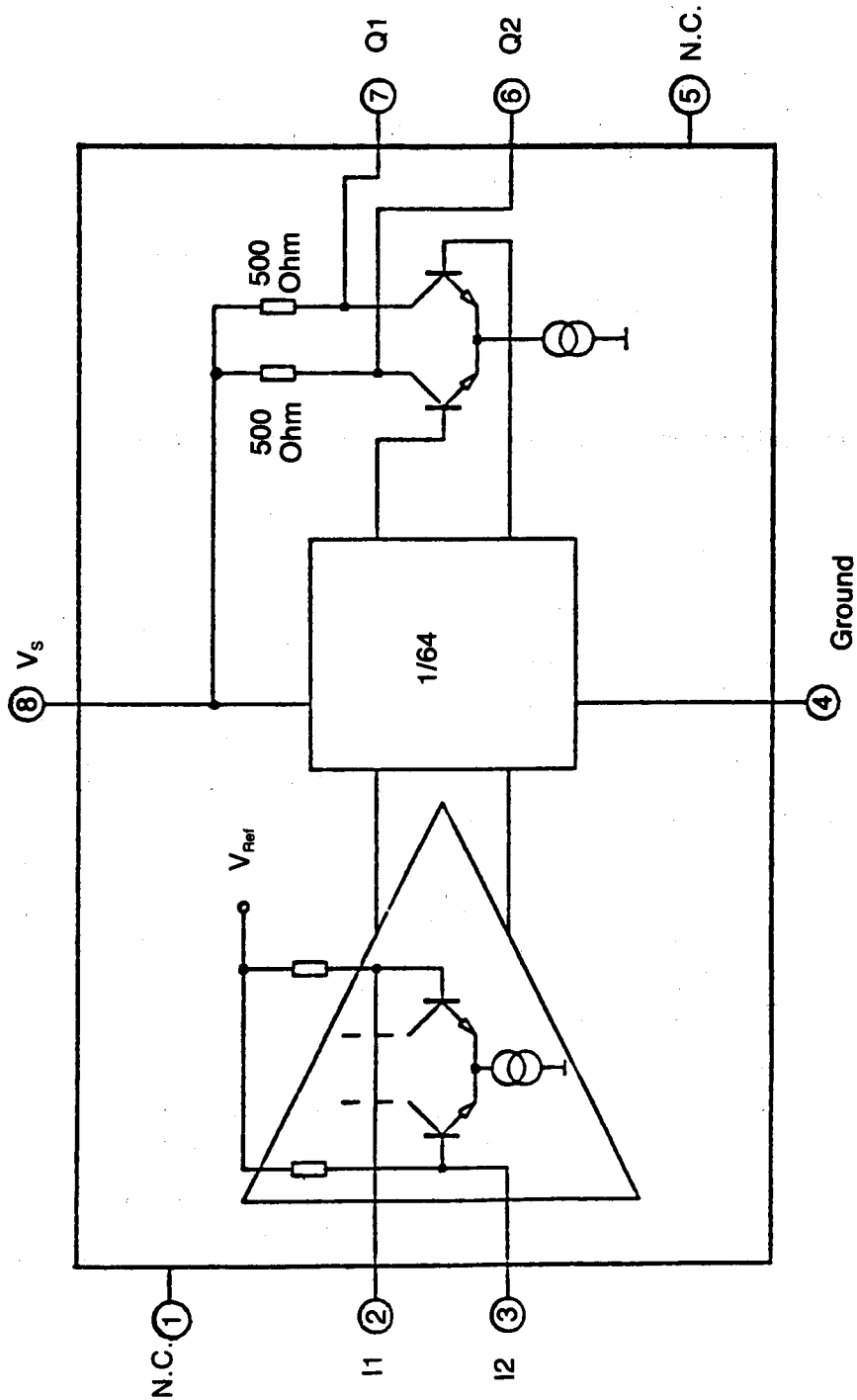
The pre-amplifier of the IC features symmetrical push-pull outputs. If one of the signal inputs is in an asymmetrical driving mode the other input should be grounded by a capacitor (≈ 1.5 nF) with low series inductivity. The pre-scaler of the IC consists of several status controlled master slave flip flops with a 1:64 scaling rate.

The asymmetrical push-pull outputs of the pre-scaler have been designed with an internal resistance of 500Ω each. The DC voltage level of the outputs is connected to the supply voltage V_S (output "high" = V_S). The typical shift is $1 V_{PP}$.

Pin configuration

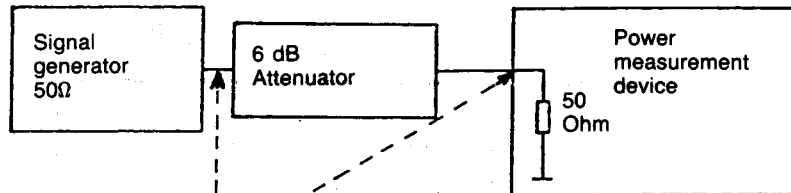
| Pin-No. | Function |
|---------|----------------------|
| 1 | N.C. |
| 2 | Input I1 |
| 3 | Input I2 |
| 4 | Ground |
| 5 | N.C. |
| 6 | Output Q2 |
| 7 | Output Q1 |
| 8 | Supply voltage V_S |

Block diagram

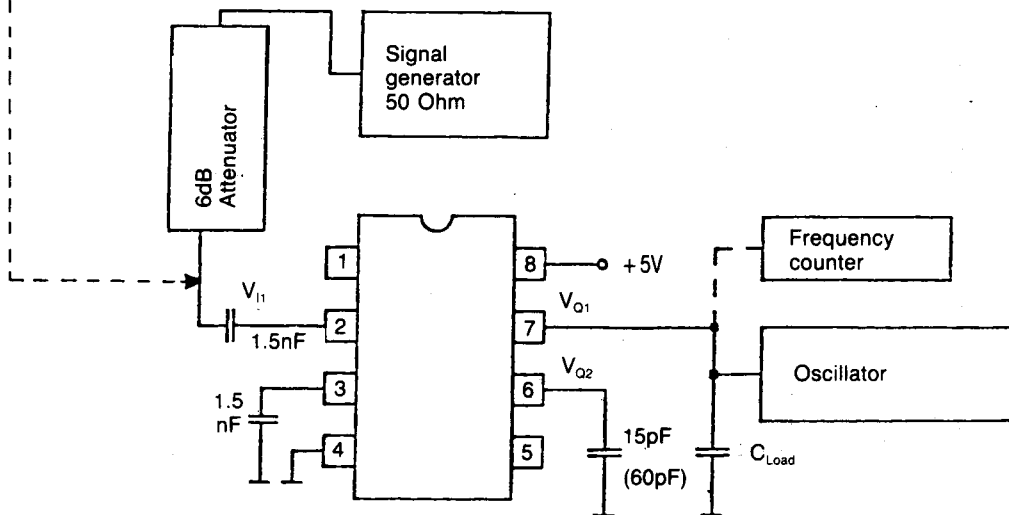


Test and measurement circuits

Signal generator calibration



Measurement configuration for input sensitivity and the output voltage swing



Test circuit 1

Capacitive load definition
for output voltage swing
measurement:
 $C_{Load} + \text{capacities of the measurement devices} = 15 \text{ pF}$
(60 pF)

Typical input sensitivity of pre-scaler

$V_S = 5\text{ V}$; $T_{amb} = 25^\circ\text{C}$

