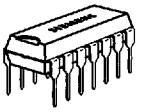
SIEMENS

PLL Frequency Synthesizer with 3-Wire Bus — TBB 206

Preliminary Data — **CMOS IC**

Features

- Serial bus (3-wire bus: data, clock, enable) for fast programming ($f_{max} \approx 1.3$ MHz)
- Modulus control
- Integrated voltage doubler for high phase detector output voltage
- High input sensitivity (100 mV), high input frequencies (90 MHz) in single-modulus operation (for $V_{DD} = 5$ V, $T_A = 25$ °C)
- Low operating current consumption (typ. 2.5 mA)
- Standby circuit
- Extremely fast phase detector with very short anti-backlash pulse
- Linearization of phase detector output by current sources
- Large division ratios for small incremental frequencies
  - A divider 0 to 127
  - N divider 3 to 4095
  - R divider 3 to 65535
- Polarity and current rate of phase detector under bus control
- Synchronous programming of dividers (N(N/A), R dividers)
- Two multifunction outputs (bus-controlled)
  - ΦR, ΦVN digital phase detector output signals (e.g. for external charge pump)
  - FRN, FVN outputs of R and N dividers
  - PRT1, 2 port outputs (e.g. for prescaler standby)
  - current external current setting for PD output
- Lock detector output (can also be read via the bus)



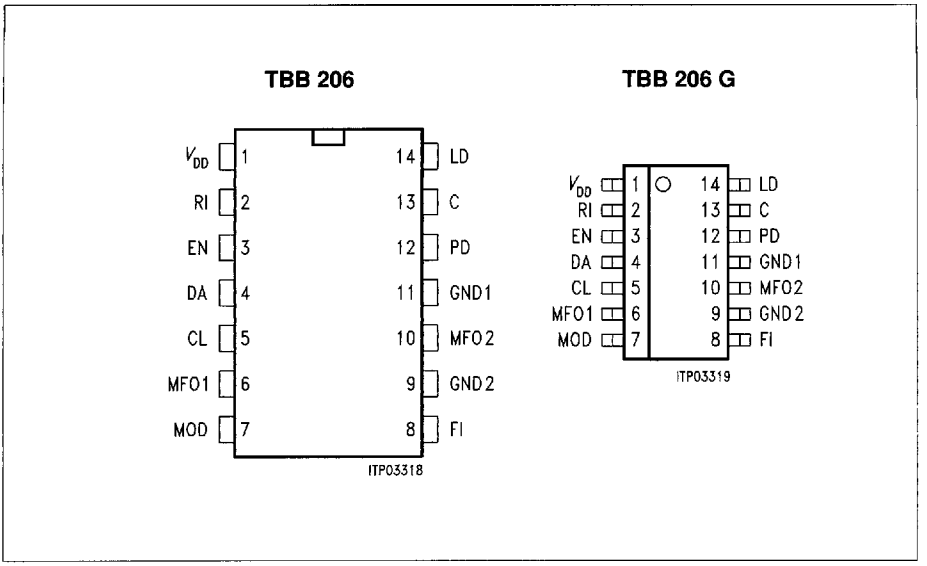
P-DIP-14-1

P-DSO-14-1

Type	Ordering Code	Package
▼ TBB 206	Q67100-H8722	P-DIP-14-1 (not for new development)
TBB 206 G	Q67100-H8723	P-DSO-14-1 (SMD)
TBB 206 G	Q67106-H8723	P-DSO-14-1 (SMD) (Tape & Reel)

TBB 206 is a CMOS integrated circuit that was specially designed for use in battery -powered radiocommunication equipment and telephones. It is suitable for both simple frequency synthesis and dual-modulus synthesis.

Pin Configurations(top view)



Pin Definitions and Functions

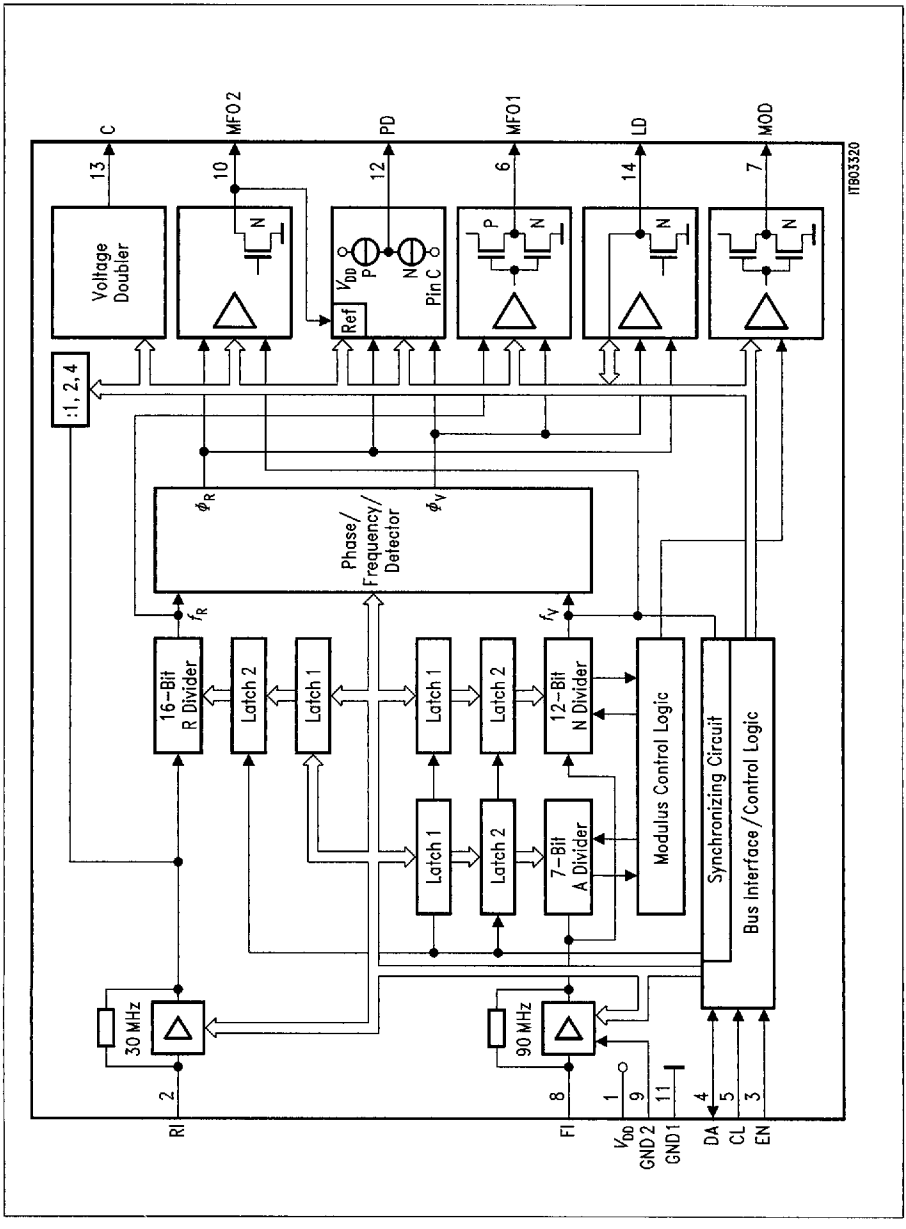
Pin No.	Symbol	Function
1	V_{DD}	Supply voltage
2	RI	**Input for 16-bit R Divider** (reference divider). The input has a sensitive preamplifier. AC coupling should be provided for small input signals, DC coupling being possible for large input signals.
3	EN	**Enable Line of 3-Wire Bus.** When EN = High, the input signals CL and DA of the three-line bus are disabled internally. EN = Low activates the bus control. The internal (received) data of the DA line are transferred into the latches with the positive edge of the EN signal.
4	DA	**Serial Data Input of 3-Wire Bus.** The number of data is dependent on the required programming (see transmission protocols). The last three bits before the EN signal define where the transmitted data are to be assigned. In byte-oriented data structure the data are to be transmitted justified to the EN signal, i.e. bits to be filled in (don't care) are transmitted first.
5	CL	**Clock Line of 3-Wire Bus.** The serial data are read into the internal shift registers with the positive edge (i.e. appear on the output of the shift register).

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>6/10</td><td>MFO1/2</td><td>Multifunction Outputs 1/2. Various functions can be assigned to the outputs via the bus (see programming). MFO2 is an open-drain n-channel output and has higher voltage capability than the other outputs of TBB 206. This offers the possibility of driving external stages with higher operating voltages. The signals ΦR and ΦVN are the digital output signals of the phase and frequency detector and are inverted to one another. In this way external, active current sources (for greater currents) can be driven directly.
$f_V < f_R$ or f_V lagging: Φ_R active low
$f_V > f_R$ or f_V leading: Φ_{VN} active high
$f_V = f_R$ and PLL locked in: Φ_R high-impedance, Φ_{VN} low
The signals FRN and FVN are the scaled down signals of RI and FI. The low time corresponds to $1/f_{RI}$ and $1/f_{FI}$ respectively.
MFO2 can be used as an input for current setting of the PD output. A positive current is to be fed in for this purpose. The bus control for stepping down is maintained. The assignment of the output signals FRN, FVN and ΦR, ΦVN to the input signals FI, RI can be exchanged by status 2, bit 3 (PD polarity).
In the PORT function the outputs are assigned to the access of the status progamming. The outputs react with the rising edge of the EN signal. The standby mode does not affect the PORT function. The following statuses
<table>
<tr><th>Status</th><th>MFO1
push-pull</th><th>MFO2
open-drain</th></tr>
<tr><td>FRN/FVN</td><td>low</td><td>high-impedance</td></tr>
<tr><td>ΦR/ΦVN</td><td>low</td><td>high-impedance</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>MOD</td><td>Modulus Control Output for External Dual-Modulus Prescaler. The modulus output is low at the beginning of the cycle. When the A divider has reached its set value, MOD goes high. When the N divider has reached its set value, MOD goes low again and the cycle starts again. If the prescaler has the divider factors P or P + 1 (P for MOD = high, P + 1 for MOD = low), the total division factor is N × P + A. The value of the A divider must be smaller than that of the N divider.
In single-modulus operation and standby in dual-modulus operation the output is high-impedance for open-drain and tristate for push-pull.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
8	FI	**VCO Frequency**. Input with highly sensitive preamplifier for 12-bit N divider and 7-bit A divider. AC coupling should be provided for small input signals, DC coupling being possible for large input signals.
9	GND2	Ground of the internal sensitive preamplifier of input FI. This must be connected externally to GND1.
11	GND1	Ground
12	PD	**Phase Detector.** Tristate charge pump output. The integrated negative and positive current sources can be programmed in current density via the bus. The activation / deactivation depends on the phase relationship of the scaled down input signals FI:N, RI:R (**see diagram 6**). $f_N < f_R$ or f_V lagging: p-channel current source active $f_N > R_R$ or f_V leading: n-channel current source active $f_N = f_R$ and PLL locked in: current sources disabled, output is high-impedance (tristate) In standby mode tristate is set. The assignment of the current sources to the output signals of the phase detector can be exchanged by status 2, bit 3 (polarity), i.e. the sign of the phase detector constant is controllable.
13	C	**Voltage Doubler Capacitor Output**. The internal, capacitive voltage doubler works into an external capacitance on pin 13 (C: + on pin 11, – on pin 13). A typical capacitance value is 1 to 10 µF. The capacitor should have low leakage currents. If the voltage doubler is not required, connect pin C to GND1. Pin 13 is at the same time the foot of the n-channel current source of the PD output. The clock frequency of the converter is derived via a programmable divider (:1, :2, :4) from the signal on RI. The internal clock frequency should be greater than 2 MHz. For V_{SS} = 5 V, f_{REF} = 25 kHz, I_{DD} = 2.0 mA, output voltage $-V_{VD}$ = 2.3 V typ.
14	LD	**Lock Detector Output** (open-drain). Unipolar output of the phase detector in the form of a pulse-width-modulated signal. In the locked-in state the Low pulse width corresponds to the anti-backlash pulse. In standby mode the output is high-impedance. The status can be scanned on the bus (status 3). Reading during standby mode is not meaningful.



Block Diagram

Circuit Description

TBB 206 is a complex PLL circuit in CMOS technology for processor-controlled frequency synthesis. Integrated, active current sources (charge pump) with programmable phase detector constants mean that the requirements of the GSM concept can be fulfilled with fast loops for example. The PLL is also notable for its flexibility and low dissipation in many different applications.

The function (Single- or Dual-modulus) and division ratios are selected on a 3-wire bus with the pins CL, DA and EN. All data (S: 50 bits, D: 57 bits) must first be transmitted for initialization. The bus interface is organized so that alterations can be executed as rapidly as possible. A change of channel requires 15 bits (S) or 22 bits (D).

TBB 206 has a standby mode for reducing current consumption. Here either the dividers or the preamplifiers can be switched off. Activation after standby is possible with the short status word (status 1:8 bits), i.e. the previously programmed division ratios and other settings are retained.

The reference frequency is fed into input RI; this may be maximally 30 MHz. The VCO frequency is applied to input FI and may be max. 90 MHz in single-modulus operation and 30 MHz in dual-modulus operation.

The PLL can be operated with or without an internal voltage doubler, depending on the required frequency variation (Varicap). The frequency (f_{VD}) is derived from RI. The divider factor is set via the 3-wire bus.

Output PD produces the phase detector signal with especially short anti-backlash pulses to avoid a dead zone and to neutralize even the smallest phase deviations. Phase differences of less than100 ps can be resolved. Output PD is configured as a current source so that the loop filter (integrator) can be designed only with passive components. The polarity and current of the PD output can be selected by the 3-wire bus. The open-drain output LD produces the lock-detect signal. The lock-detect output can be read via the bus.

The function of the multifunction outputs MFO1, MFO2 can be selected by status 2 programming. The outputs have four functions:

a)PRT, where PORT 1 (MFO1) is a push-pull output and PORT 2 (MFO2) an open-drain output with higher voltage capability.

b)Phase detector current continuously adjustable with external resistor R between 0.1 and 4 mA (internal reference resistor is disconnected).

c)Test outputs FVN = FI:NT, FRN = RI:RT

d)Digital switching outputs of the phase detector ΦR, ΦVN for driving external, active current sources, for example, or active filters to increase the phase detector constant.

To avoid extreme phase errors when the channel is changed, the new data for the N(N + A) and R divider are transferred synchronously with the reference frequency (FI:N) (programmable divider has reached zero). This ensures that the control operation starts with a phase difference of zero.

Absolute Maximum Ratings

$T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply voltage	V_{DD}	– 0.3		6	V	
Input voltage (except C)	V_I	– 0.3		V_{DD}+0.3	V	
Output voltage at C	V_C	$-V_{DD}$		0	V	
Output voltage (except MFO2)	V_O	GND		V_{DD}	V	
Output voltage MFO2	V_H			10	V	
Power dissipation per output	P_Q			10	mW	
Total power dissipation	P_{tot}			300	mW	
Ambient temperature	T_A	– 40		85	°C	
Storage temperature	T_{stg}	– 50		125	°C	

Operating Range

Supply voltage	V_{DD}	3	5	5.5	V	1)
Supply current						
single-modulus	I_{DD}		2.5	3.5	mA	2)
dual-modulus	I_{DD}		2	3	mA	3)
standby scaler	I_{DD}		1.5		mA	4)
standby preamp	I_{DD}			1	µA	5)
Ambient temperature	T_A	– 40		85	°C	
Output voltage MFO2	V_{QH}			8.5	V	

Notes

1) Test conditions: PLL loked, R_I = 10 MHz, V_{RI} = 500 mV (Notes 2 ... 4), V_{DD} = 5 V

2) f_I = 50 MHz, V_{FI} = 150 mV, NT, RT > 1000, without voltage doubler, $I_{PD} = I_{PD\,min}$

3) f_I = 10 MHz, V_{FI} = 500 mV, NT, RT > 1000, without voltage doubler, $I_{PD} = I_{PD\,min}$

4) f_I = 50 MHz, V_{FI} = 150 mV, NT, RT > 1000, for output wiring **refer to test circuit**

5) For output wiring **refer to test circuit**; inputs RI, FI open

$V_{IH\,min}$ (DA, CL, EN) : V_{DD} – 0.5 V

$V_{IH\,max}$ (DA, CL, EN) : V_{DD}

All pins have ESD protection to V_{DD} and GND except MFO2 (only to GND). Unused inputs should be connected to V_{DD} or GND.

Characteristics
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals DA, CL, EN						
H-input voltage	V_{IH}	0.7 × V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		0.3 × V_{DD}	V	
Slew rate	SR	2			V/µs	
Input capacitance	C_I			10	pF	
Input current	I_I			10	µA	V_I = V_{DD} = 5.5 V
Input Signal RI						
Input frequency	f_I			30	MHz	V_{DD} = 4.5 V
Input voltage	V_I				mVrms	(sine)*see diag.19&20
Slew rate	SR	2			V/µs	
Input capacitance	CI			10	pF	
Input current	I_I			10	µA	V_I = V_{DD}
Input frequency	f			20	MHz	V_{DD} = 3 V
Slew rate	SR	2			V/µs	
Input Signal FI (Dual modulus)						
Input frequency	f_I	0.1		30	MHz	V_{DD} = 4.5 V
Input voltage	V_I	50			mVrms	(sine)
Slew rate	SR	2			V/µs	
Input capacitance	C_I			10	pF	
Input current	I_I			10	µA	V_I = V_{DD}
Input frequency	f_I	0.1		18	MHz	V_{DD} = 3 V
Slew rate	SR	2			V/µs	

* Input voltage (see diagrams in appendix).

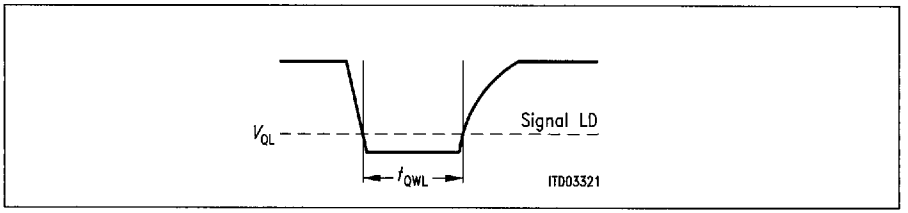
Characteristics (cont'd)
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signal FI (Single modulus)						
Input frequency	f_I	0.1		90	MHz	V_{DD} = 5 V
Input voltage	V_I				mVrms	(sine)*)**)
Slew rate	SR	2			V/µs	
Input capacitance	C_I			10	pF	
Input current	I_I			10	µA	$V_I = V_{DD}$
Input frequency	f_I	0.1		20	MHz	V_{DD} = 3 V
Slew rate	SR	2			V/µs	
Input Signal MFO2 (external PD current setting, function : current, PD current bits :0, 1)						
Input current	I_I		55		µA	V_{DD} = 5 V, I_{PD} typ. 1 mA (see diagrams in appendix)
Input voltage	V_I			***)	V	V_{DD} = 5 V
Output Signal PD (tristate output)*						
Output current (externally adjusted)	I_Q			± 4	mA	V_{DD} = 5 V
Current mode 0.25 mA	I_Q	– 35%	± 0.25	+ 35%	mA	T_A = – 25 to 60 °C
Current mode 0.5 mA	I_Q	– 35%	± 0.5	+ 35%	mA	
Current mode 1.0 mA	I_Q	– 35%	± 1.0	+ 35%	mA	
Current mode 2.0 mA	I_Q	– 35%	± 2.0	+ 35%	mA	
Tristate	I_Q			± 50	nA	
Current mode 2.0 mA	I_Q		see appendix		mA	V_{DD} = 3 V
Saturation voltage, current mode			see appendix		V	0.25 ... 2 mA
Tristate current ****)	I_Q	– 5	0	+ 5	nA	

*) Input voltage (see diagrams in appendix).
**) Guarenteed values see diagram 22
***) See diagrams 14-16
****) Guarenteed by design; not measured in production

Characteristics (cont'd)
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

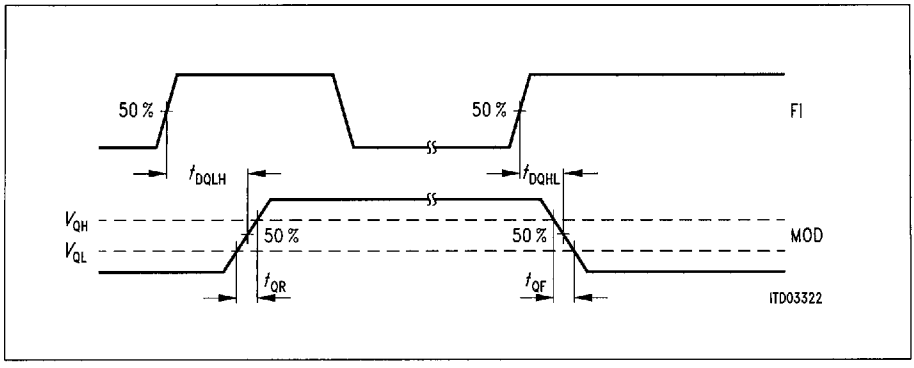
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal MFO1 (Push pull)						
H-output voltage	V_{QH}	V_{DD} – 1			V	I_{QH} = 2 mA, V_{DD} = 5 V
L-output voltage	V_{QL}			1	V	I_{QL} = 2 mA, V_{DD} = 5 V
Output Signal MFO2 (N-channel open drain)						
L-output voltage	V_{QL}			1	V	I_{QL} = 2 mA, V_{DD} = 5 V
H-output current	I_{QH}			1	µA	V_{QH} = V_{DD} + 3 V, V_{DD} = 5 V
Output Signal MOD (Push pull)						
H-output voltage	V_{QH}	V_{DD} – 0.4			V	I_{QH} = 0.5 mA, V_{DD} = 5 V
L-output voltage	V_{QL}			0.4	V	I_{QL} = 0.5 mA, V_{DD} = 5 V
Output Signal MOD (N-channel open drain)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 0.5 mA, V_{DD} = 5 V
Output Signal DA (N-channel open drain)						
L-output voltage	V_{QL}	0.4			V	I_{QL} = 3 mA, V_{DD} = 5 V, C_L = 400 pF
Output Signal LD (N-channel open drain)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 3 mA V_{DD} = 5 V C_L = 30 pF
L-output pulse width	t_{QWL}		20	40	ns	PLL locked, status 2, bit 6 = 0



Pulse Diagram

Characteristics (cont'd)
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Voltage Doubler						
Output voltage	V_{QC}	$-V_{DD}$+0.8		V_{DD}	V	f_{VD} = 2 MHz I_{QC} = 0 µA V_{DD} = 5 V PLL locked
	V_{QC}	$-V_{DD}$+1.5		V_{DD}	V	f_{VD} = 2 MHz I_{QC} = 100 µA V_{DD} = 5 V PLL locked
Current consumption	I_{VD}		250		µA	V_{DD} = 5 V I_{QC} = 0 µA f_{VD} = 2 MHz PLL locked
Output Signal MFO1, MFO2 (Function: FVN, FRN, OR, OVNPRT)						
Rise time (push pull)	t_{QR}			10	ns	C_L = 30 pF
Fall time (open drain, push pull)	t_{QF}			10	ns	C_L = 30 pF
Output Signal MOD (Push pull)						
Rise time	t_{QR}			10	ns	C_L = 30 pF
Fall time	t_{QF}			10	ns	C_L = 30 pF
Delay time L-H to FI	t_{DQLH}			25	ns	C_L = 30 pF, 5 V
Delay time H-L to FI	t_{DQHL}			15	ns	C_L = 30 pF, 5 V
Delay time L-H to FI	t_{DQLH}			42	ns	C_L = 30 pF, 3 V
Delay time H-L to FI	t_{DQHL}			25	ns	C_L = 30 pF, 3 V



Pulse Diagram

Programming

Programming of the dividers and status control are performed on a 3-wire bus. The assignment of the content of the telegrams to the functional units is made with a target address that is transmitted in the last three bits of the telegram before the EN signal.

In addition to the assignment data, the target address also contains status information: single/ dual-modulus and synchronous/asynchronous data transfer.

The following addresses are valid:

... 001 EN: status 1
... 010 EN: status 2
... 011 EN: status 3

... 110 EN: N divider = single-modulus
... 111 EN: N/A divider = dual-modulus

... 101 EN: R divider + synchronous transfer
... 100 EN: R divider + asynchronous transfer

The decision single-/dual-modulus is made simultaneously with the programming of the N or N/A divider.

Target address 000 is reserved for testing purposes.

In TBB 206 there is provision for new programming of the dividers synchronously with the reference frequency. This ensures that the control loop starts from the momentary status of the phase detector when a frequency/channel is altered. In the lock-in situation in particular, the control operation starts with a phase difference of zero. Thus there is no possibility of brief error signals at the phase detector, as they can occur in asynchronous data transfer.

In **asynchronous** programming the "new" data are transferred asynchronously to the status of the R, N (N/A) divider into intermediate registers L2. There is no guarantee that all data, i.e. R and N(N/A) dividers, will be present in time, so this will result in additional error signals at the phase detector intput .

Programming

Synchronous programming offers the possibility of data transfer while maintaining the phase difference that exists at the time of (internal) programming. This is done as follows:

1. **Setting** of the mode "synchronous transfer" by appropriate programming of the R divider. This setting is maintained until programmed differently. With the EN of the R-divider programming the "new" data are only read into capture register L1.
2. **Programming** of the N or N/A divider. With the EN signal of the programming the "new" data are likewise only read into capture register L1. At the same time synchronous transfer into intermediate register L2 is primed for all dividers. This transfer is then made with the next zero crossing of the particular divider. A phase difference existing at the instant of transfer is maintained, this being the start condition for the further control operation, based on the "newly" read data.

Because of the synchronizing circuit, the delay in data transfer is maximally $2 \times 1/f_{REF}$.

The synchronous programming operation is always initiated by the EN signal of the N or N/A divider and also applied to the R divider, even if its data have not been altered. If the data content of the R divider (e.g. for a change of reference frequency) is to be altered, this consequently has to be done before programming of the N or N/A divider.

Synchronous transfer is of particular advantage if extreme channel jumps are to be made with short settling time. For fast "coarse" settling a switch is made to a greater reference frequency, thus increasing the bandwidth of the loop. The original reference frequency is returned to when the "quasi-set" status is reached. Control to the "actual" value is tmade with the known settling response for small channel jumps. Synchronous transfer ensures that no extra phase errors occur as a result of changing the reference frequency.

Programming: Times

Initialization, sequence: R divider before N divider

Single-modulus:	Σ 50 bits	Dual-modulus:	Σ 57 bits
Status 2	16 bits	Status 2	16 bits
R divider	19 bits	R divider	19 bits
N divider	15 bits	N/A divider	22 bits

Change of channel, at same reference frequency

Single-modulus	15 bits
Dual-modulus	22 bits

If the reference frequency is altered, the R divider also has to be loaded (+ 19 bits).

Maximum repetition rate for channel Change f_{FI}:N.

Note:
After Power on initializing routine according to the pulse diagram p. 18 is necessary.

Programming: Tables

Status Bit		Multifunction Outputs	
MFO 1	MFO 2	MFO 1 (push pull)	MFO 2 (open-drain N)
0	0	FRN	FVN
0	1	ΦVN	ΦFR
1	0	PRT 1	PRT 2
1	1	PRT 1	Current *

* Input

Status Bit		PD Output Current
PD Current 1	PD Current 2	typ. (mA)
0	0	0.25
1	0	0.5
0	1	1.0
1	1	2.0

Status Bit		Voltage-Doubler Frequency
Voltage Doubler		f_{INT}
1	2	
0	0	OFF
1	0	R_I: 1
0	1	R_I: 2
1	1	R_I: 4

Programming: Transmission Protocol

Status 1

	MFO1	
	MFO2	
	PD polarity	
	Modulus output	
	Preamplifier (standby)	
	Anti-backlash pulse	
	Voltage doubler 1	
	Voltage doubler 2	
1	PORT 1	
2	PORT 2	
3	Divider (standby)	
4	PD current 1	
5	PD current 2	
6	0	0
7	0 Target address	1
8	1	0
EN		

Status 2*

	0	1
1		See
2		table
3	neg.	pos.
4	push-pull	open drain
5	standby	active
6	20 ns	40 ns
7		See
8		table
9	0**	1**
10	0**	1**
11	standby	active
12		See
13		table
14		
15		
16		
EN		

Status 3: Lock Detector Read

1	0
2	1 Target address
3	1
EN	Status lock detect: lock-in = low***
1	
EN	

* Status 2 must always be used to initialize
(Bit 1-8 of status 2 have no default values).

** Only valid if multifunction outputs are in PORT status, otherwise don't care.

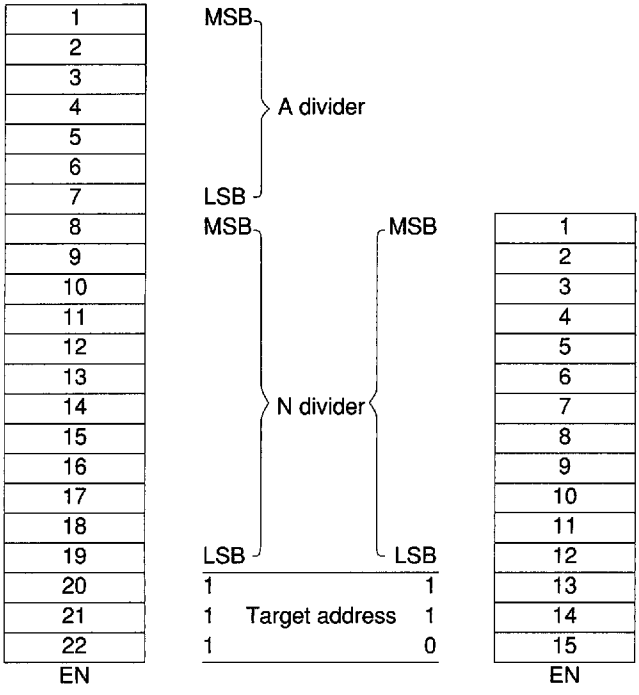
*** DA of TBB 206 can only produce low (open-drain output).

N/A Divider

N Divider

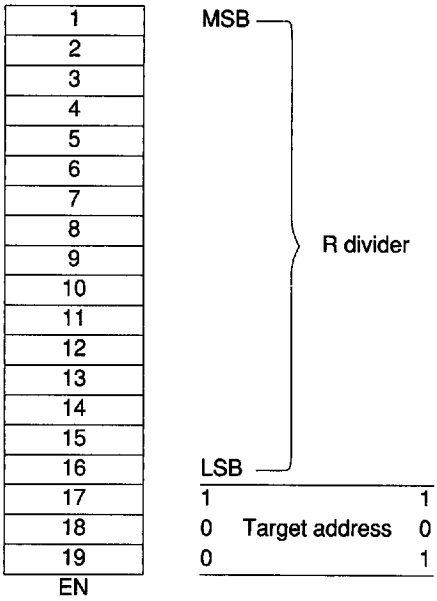
Dual Modulus

Single Modulus



Address 111: dual modulus
Address 110: single modulus

R Divider



Address 111: synchronous transfer*
Address 110: asynchronous transfer*

* Also determines transfer mode for N, N/A divider.

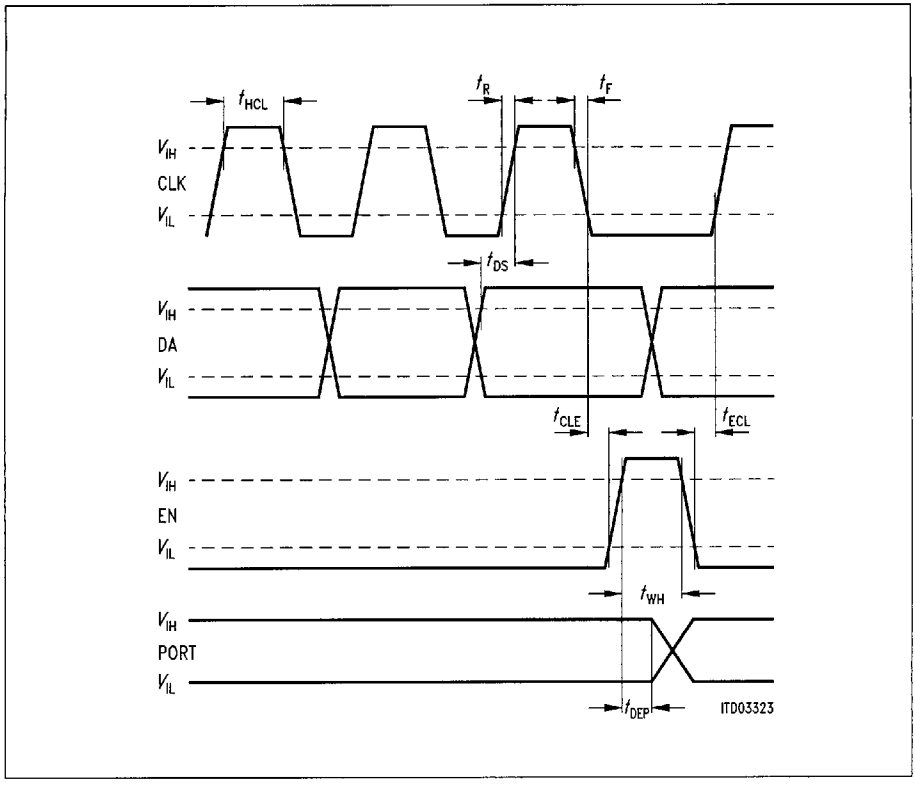


Diagram 1
Timing Diagram for 3-Wire Bus

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{CL}		1.3	MHz
H-pulse width (CL)	t_{HCL}	400		ns
Data setup	t_{DS}	100		ns
Setup time clock-enable	t_{CLE}	5		ns
Setup time enable-clock	t_{ECL}	100		ns
H-pulse width (enable)	t_{WH}	80		ns
Transition time	t_R, t_F		10	µs
Delay time enable port	t_{DEP}		1	µs

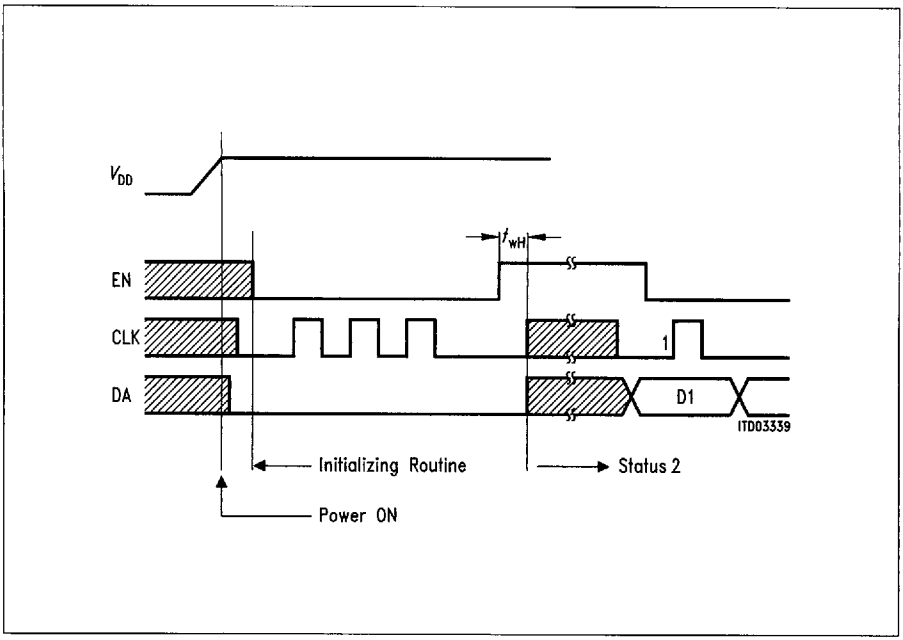


Diagram 2
Initializing Routine after Power ON

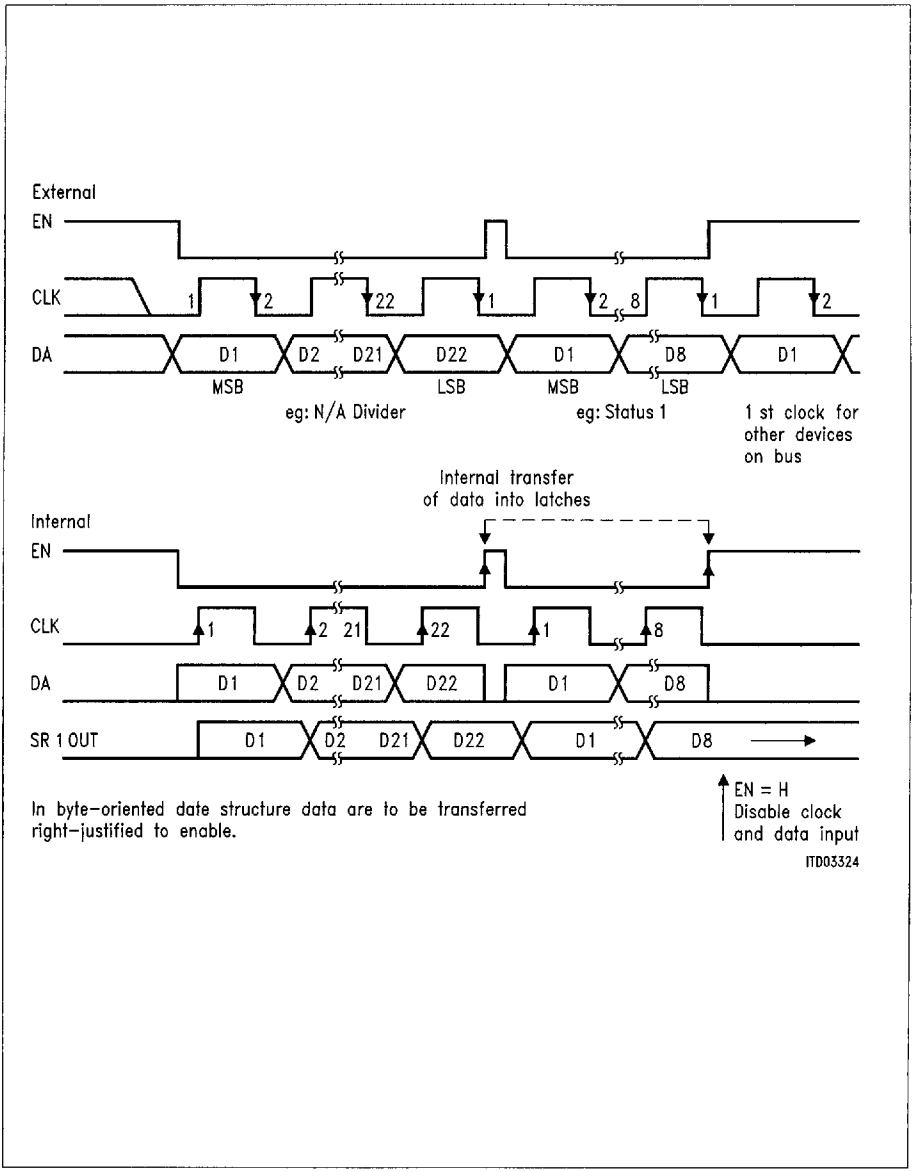


Diagram 3
Pulse Diagram for 3-Wire Bus

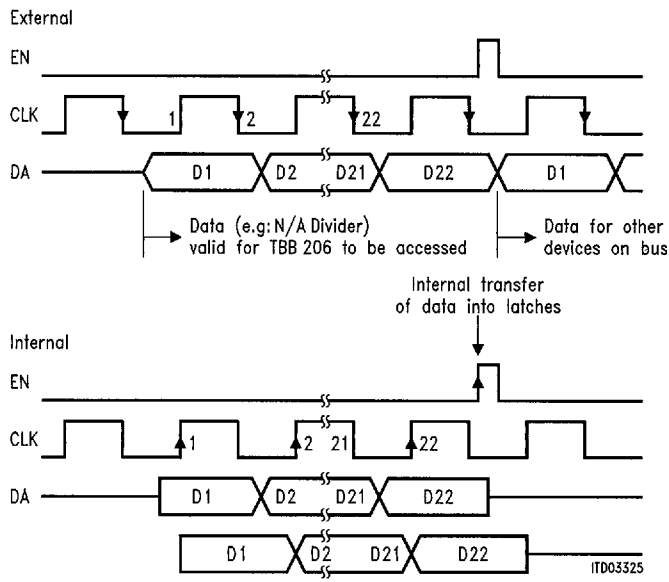


Diagram 4
Pulse Diagram for 3-Wire Bus "Dynamic" EN Control

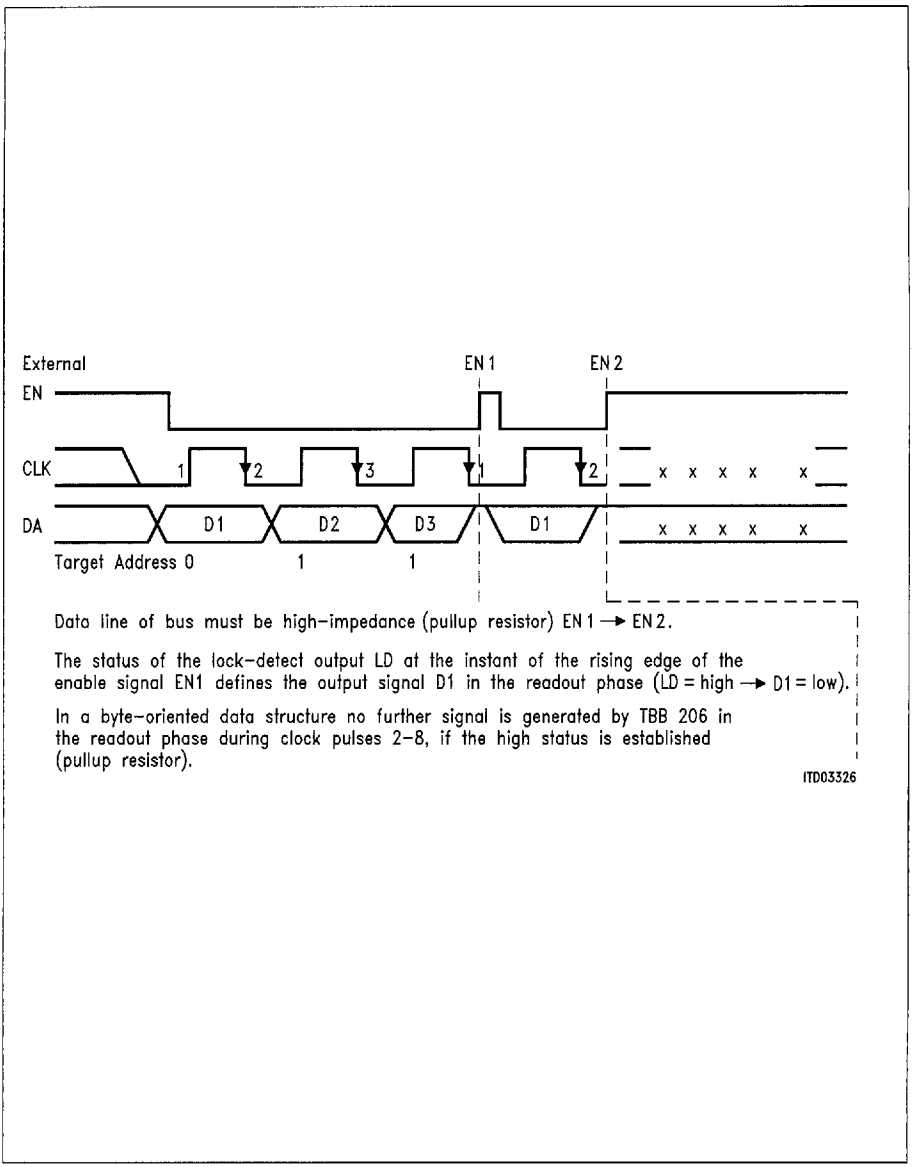


Diagram 5
Pulse Diagram for 3-Wire Bus Read Lock Detector

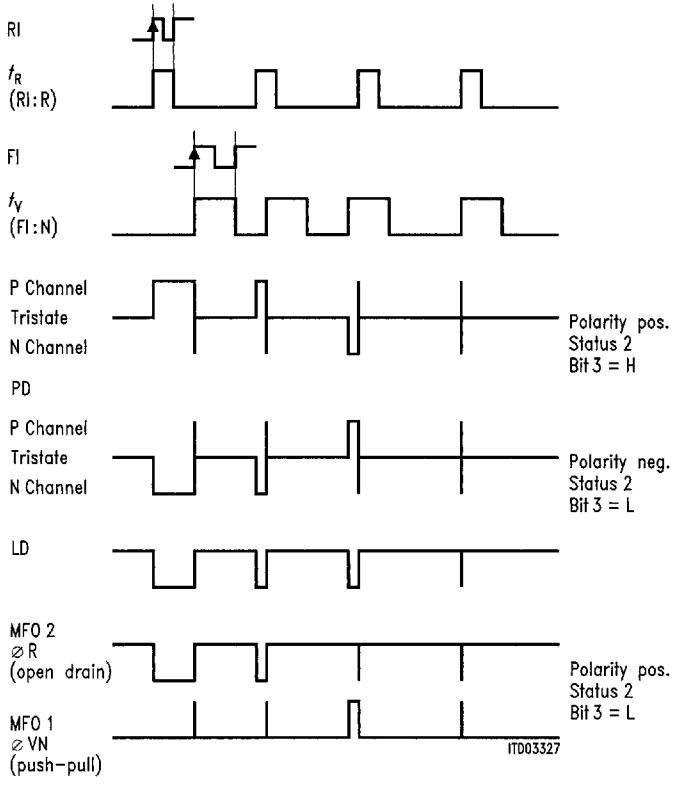
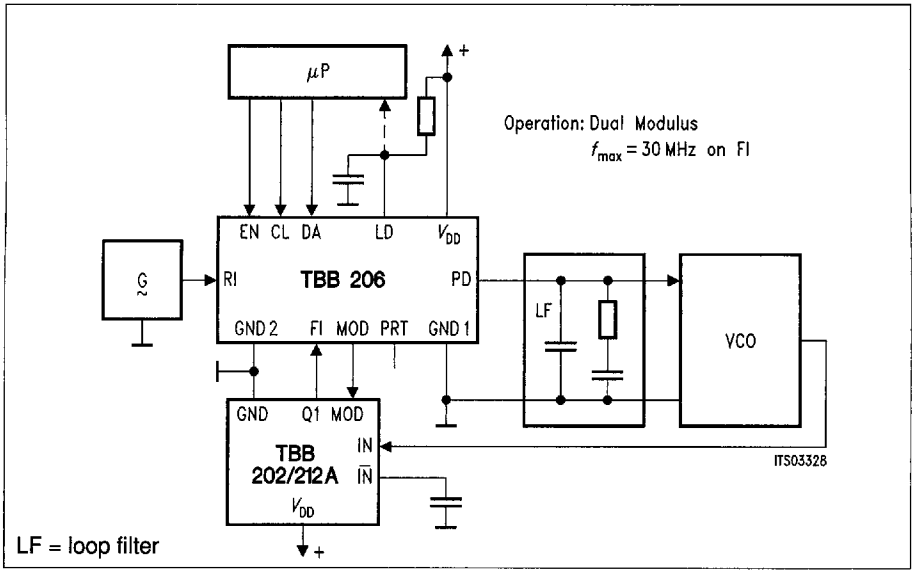
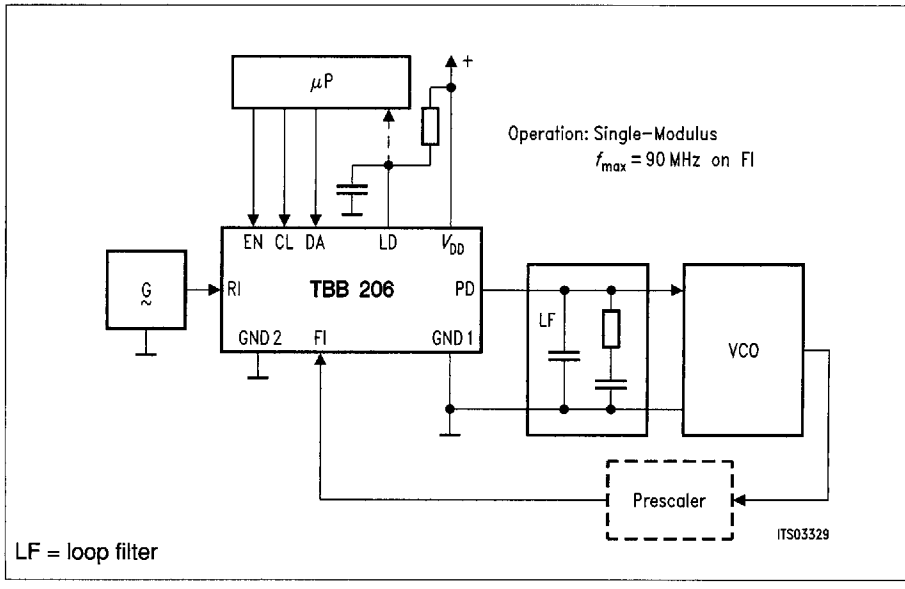


Diagram 6
Phase Detector / Lock Detector

Application Circuits

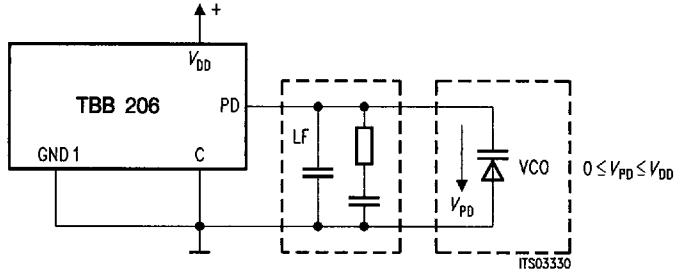


Select appropriate divider ratios of dual-modulus prescaler 128/129 or 64/65 according t
reference frequency.



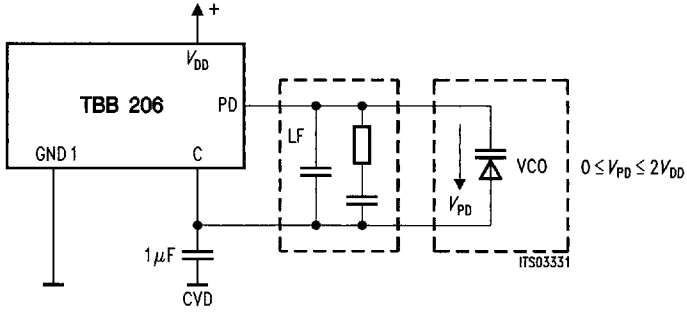
Application Circuits

VCO Coupling



LF = Loop Filter

Operation without Voltage Doubler (status bit = see tables programming)

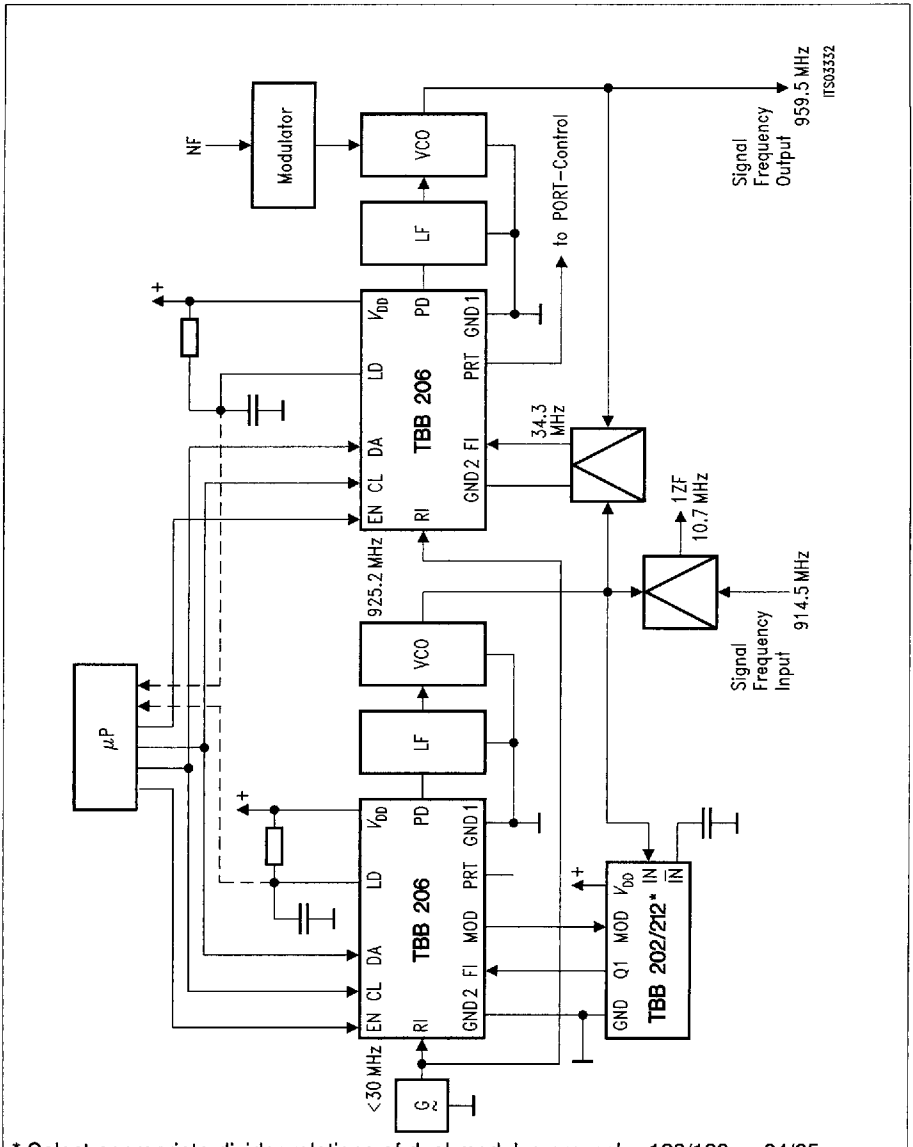


LF = Loop Filter

Operation without Voltage Doubler (status bit = see tables programming)

Application Circuit

900 MHz Range



* Select appropriate divider relations of dual-modulus prescaler 128/129 or 64/65 according to reference frequency.

Appendix

Input Sensitivity of Preamplifier
Test Circuit and Test Procedure

Test procedure:

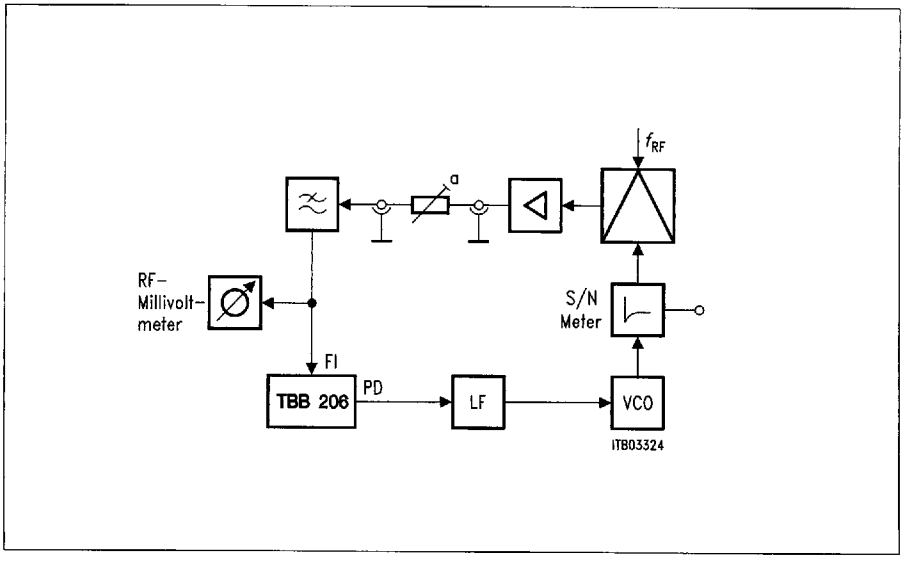
1. Determine S/N ratio of VCO with CCITT weighting:

   Input level on FI: 0 dBm
   Input frequency on FI: $f_{VCO} - f_{RF}$

2. Increase attenuation until – 3 dB point is reached.

   Sensitivity = input level on FI

   Boundary condition:
   The bandwidth of the control loop must be substantially higher than the upper cutoff frequency of the CCITT filter. Measure without LD circuitry; bus inactive.



Test Circuit

Diagram 7

PD Output Curve $I_{N\ channel}$ (typ.), V_{DD} = 5 V, I_{PD} range = 2 mA

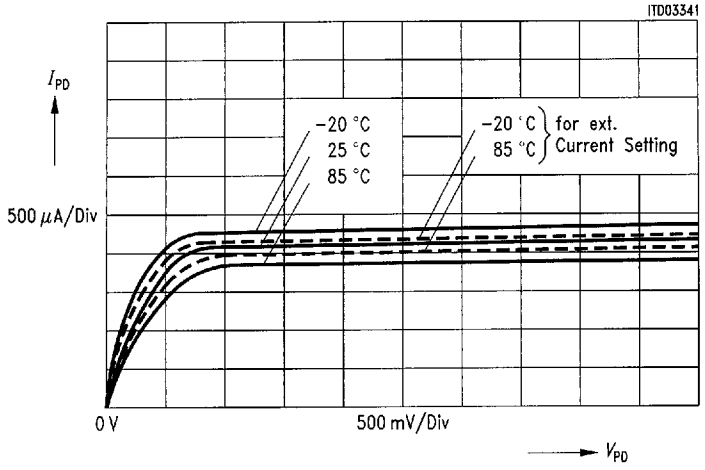


Diagram 8

PD Output Curve $I_{P\ channel}$ (typ.), V_{DD} = 5 V, I_{PD} range = 2 mA

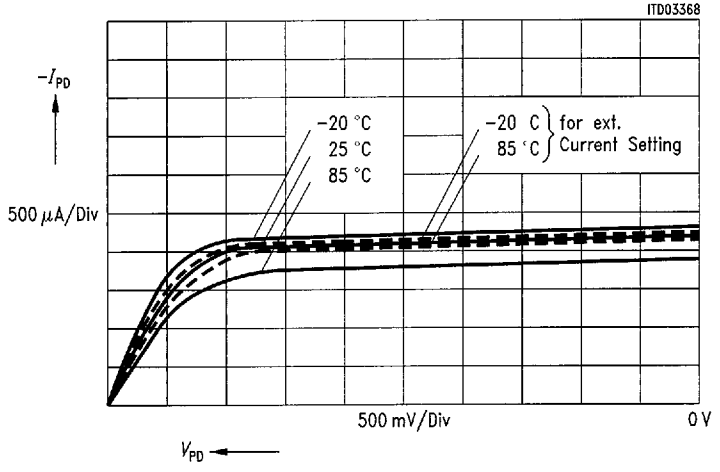


Diagram 9

PD Output Curve $I_{N\ channel}$ (typ.), V_{DD} = 5 V, T_A = 25 °C

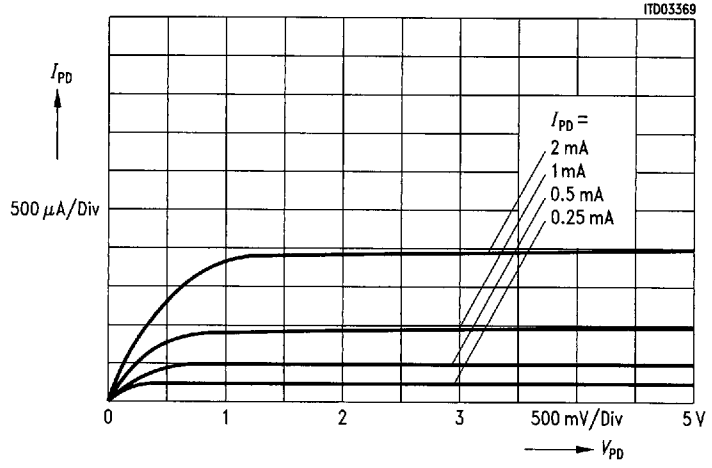


Diagram 10

PD Output Curve $I_{P\ channel}$ (typ.), V_{DD} = 5 V, T_A = 25 °C

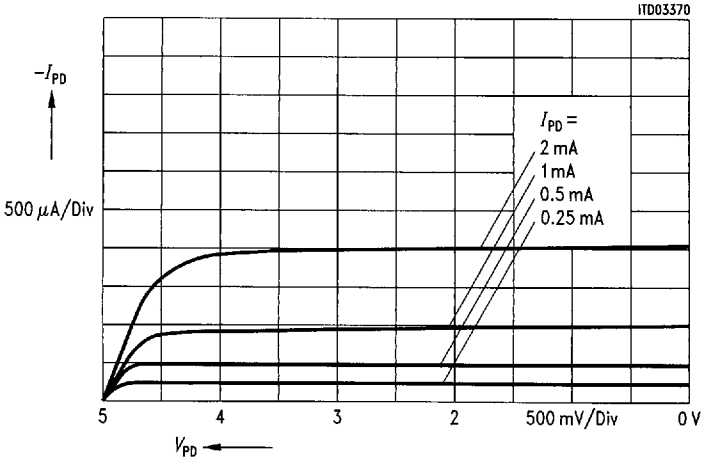


Diagram 11

PD Output Curve $I_{N\ channel}$ vs V_{DD} (typ.), T_A = 25 °C, I_{PD} = 2 mA

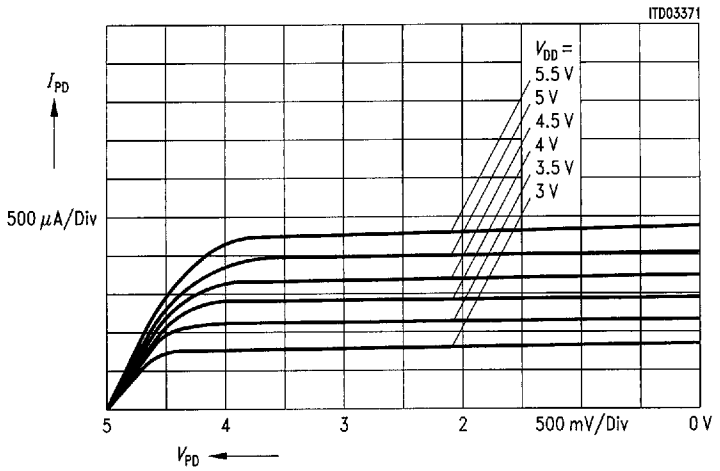


Diagram 12

PD Output Curve $I_{P\ channel}$ vs V_{DD} (typ.), T_A = 25 °C, I_{PD} = 2 mA

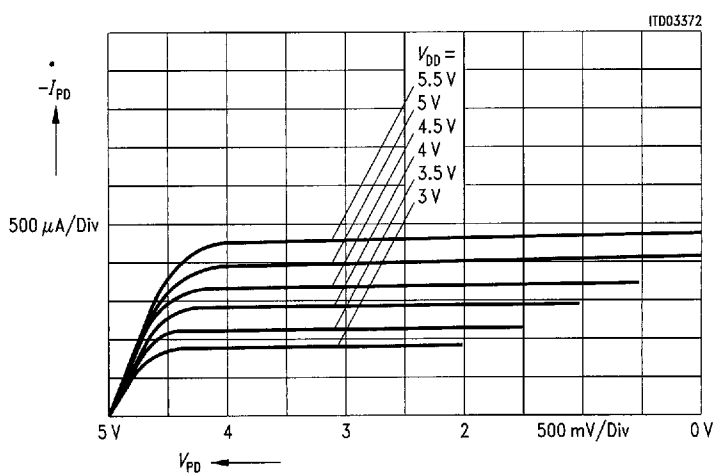


Diagram 13

I_I : I_{PD} Ratio (typ.), T_A = 25 °C, V_{DD} = 5 V
(external PD current setting on M_{FO2})

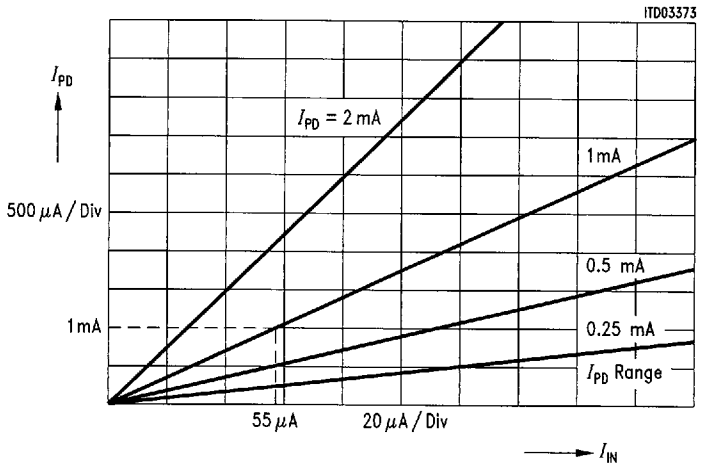


Diagram 14

External PD Current Setting on M_{FO2}, Temperature Effect on I_I (typ.) V_{DD} = 5 V

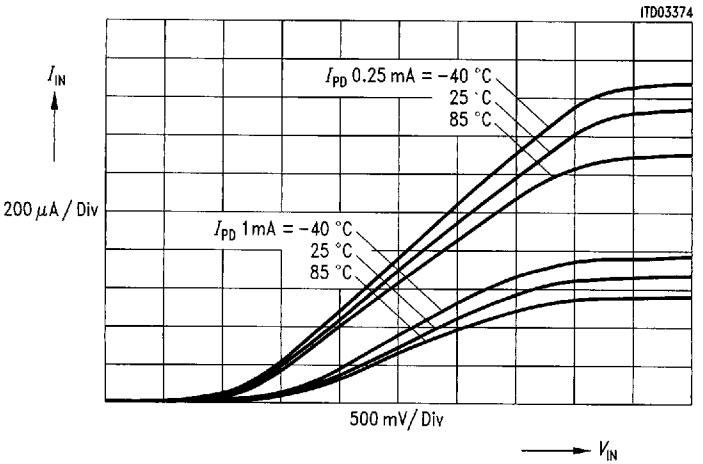


Diagram 15

I_I in Relation to Selected Current Range (typ.)
(external current setting on M_{FO2})

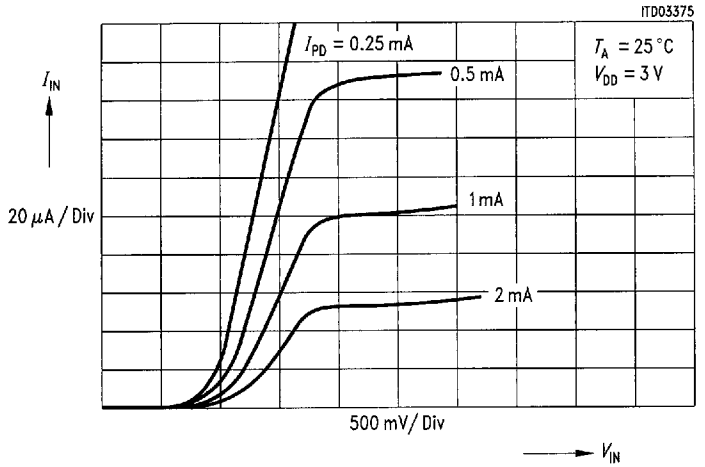


Diagram 16

I_I in Relation to Selected Current Range (typ.)
(external current setting on M_{FO2})

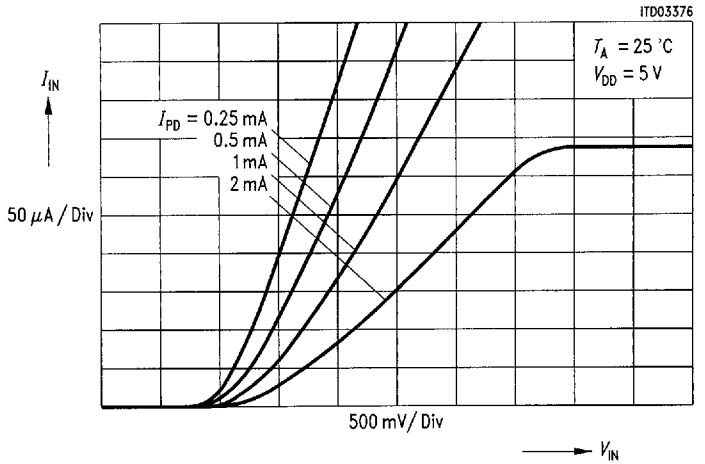


Diagram 17

I_I : I_{PD} Ratio (typ.), T_A = 25 °C, V_{DD} = 3 V
(external PD current setting on M_{FO2})

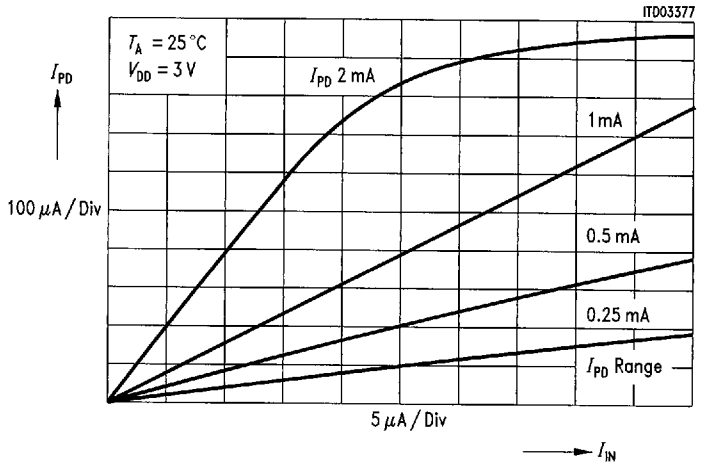


Diagram 18

I_I : I_{PD} Ratio (typ.), T_A = 25 °C, V_{DD} = 5 V
(external current setting on M_{FO2})

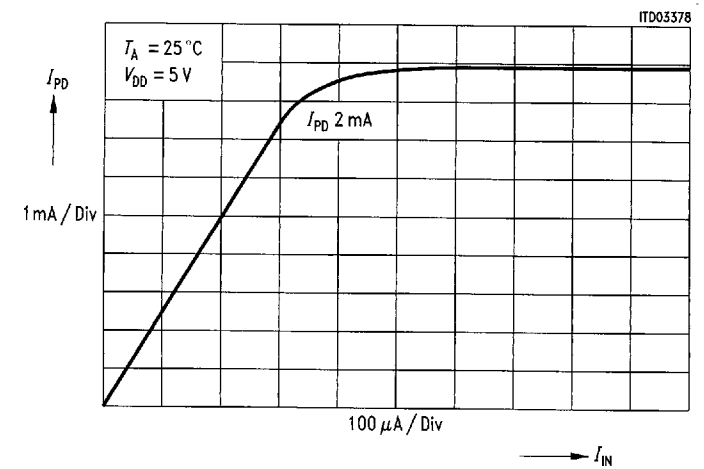


Diagram 19

Input Sensitivity (typ.) of RI Input
T_A = 25 °C, V_{DD} = 5 V

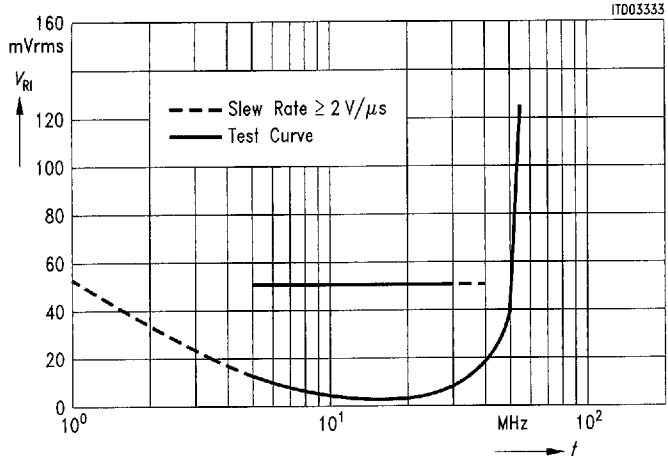


Diagram 20

Input Sensitivity Single Modulus (typ.) of FI Input
T_A = 80 °C, V_{DD} = 3 V

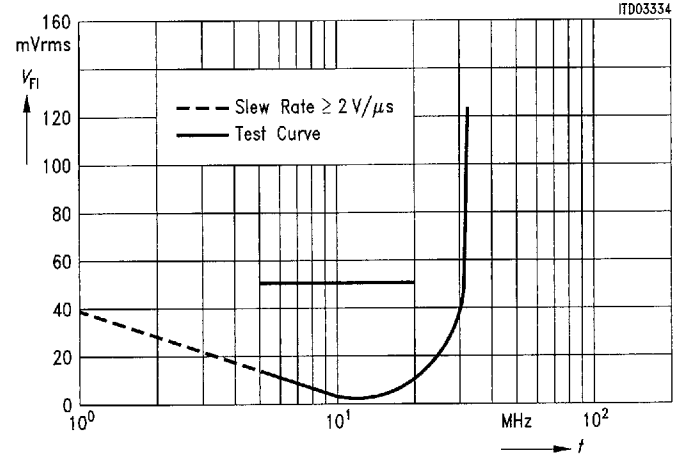


Diagram 21

Input Sensitivity Single Modulus (typ.) of FI Input
T_A = 25 °C

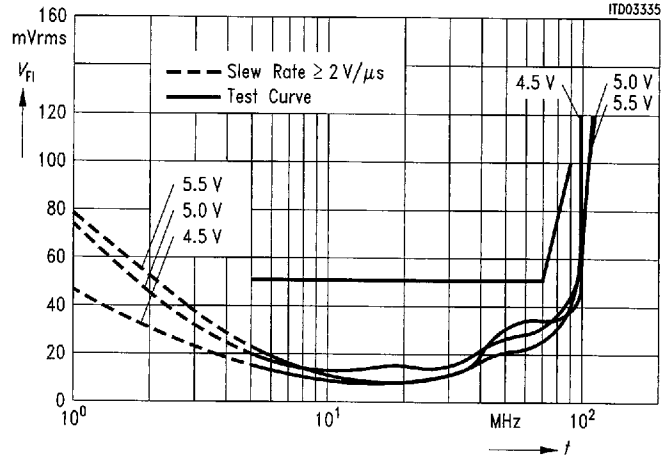


Diagram 22

Input Sensitivity Single Modulus (typ.) of FI Input
V_{DD} = 5 V

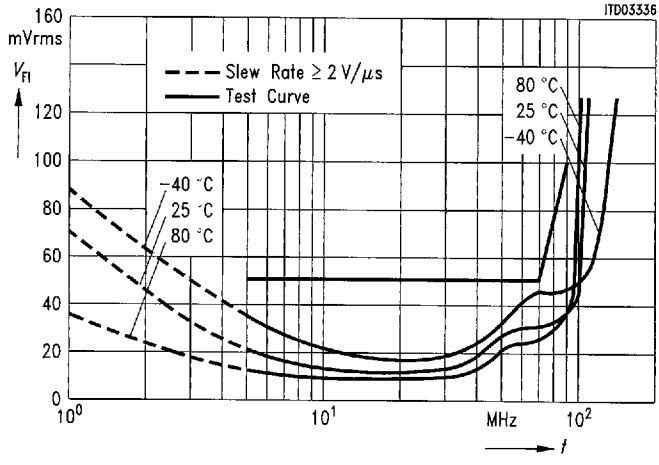


Diagram 23

Input Sensitivity Single Modulus (typ.) of FI Input
T_A = 25 °C, V_{DD} = 3 V

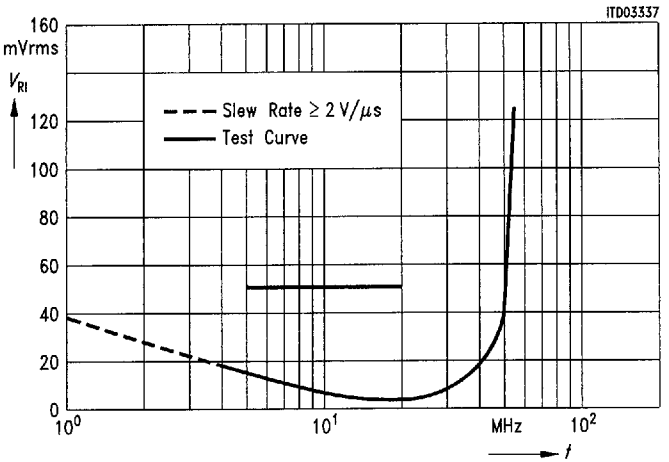
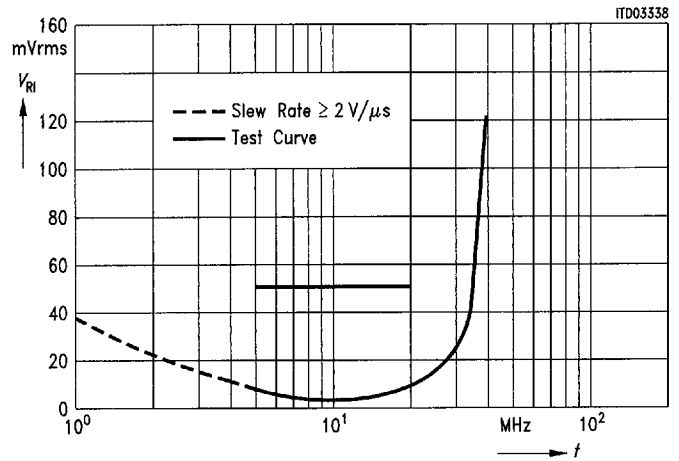
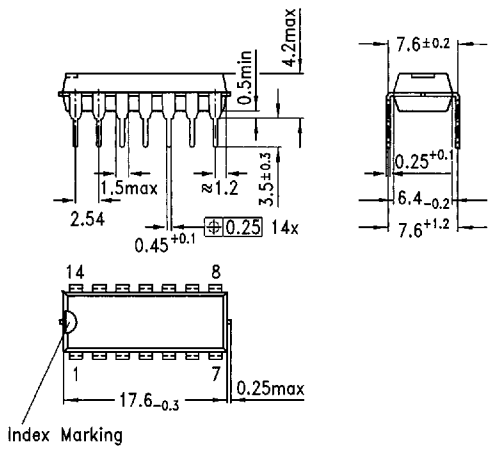


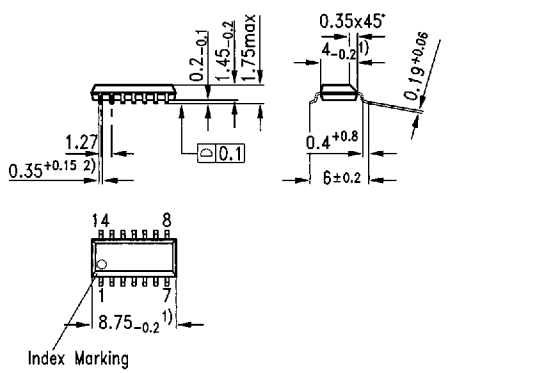
Diagram 24
Input Sensitivity (typ.) of RI Input
T_A = 25 °C, V_{DD} = 3 V



Plastic Package, P-DIP-14-1
(Dual-In-Line)



Plastic Package, P-DSO-14-1 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm