

# **Surface Mount PIN Diodes**

# **Technical Data**

**HSMP-386x Series** 

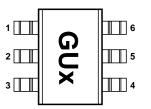
### **Features**

- Unique Configurations in Surface Mount Packages
  - Add Flexibility
  - Save Board Space
  - Reduce Cost
- Switching
  - Low Distortion Switching
  - Low Capacitance
- Attenuating
  - Low Current Attenuating for Less Power Consumption
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Low Failure in Time (FIT) Rate<sup>[1]</sup>

### Note:

1. For more information see the Surface Mount PIN Reliability Data Sheet.

## Pin Connections and Package Marking, SOT-363



### Notes:

- 1. Package marking provides orientation, identification, and date code.
- 2. See "Electrical Specifications" for appropriate package marking.

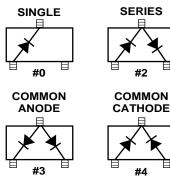
## **Description/Applications**

The HSMP-386x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance is the driving issue for the designer.

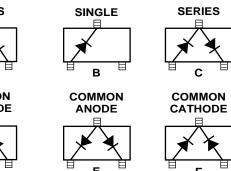
The HSMP-386x series Total Capacitance ( $C_T$ ) and Total Resistance ( $R_T$ ) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383x series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

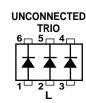
## Package Lead Code Identification, SOT-23 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



## Absolute Maximum Ratings<sup>[1]</sup> $T_C = +25^{\circ}C$

Symbol	Parameter	Unit	SOT-23	SOT-323
If	Forward Current (1 µs Pulse)	Amp	1	1
P <sub>IV</sub>	Peak Inverse Voltage	V	50	50
Tj	Junction Temperature	°C	150	150
T <sub>stg</sub>	Storage Temperature	°C	-65 to 150	-65 to 150
$\theta_{jc}$	Thermal Resistance <sup>[2]</sup>	°C/W	500	150

*ESD WARNING:* Handling Precautions Should Be Taken To Avoid Static Discharge.

#### Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.

2.  $T_C$  = +25°C, where  $T_C$  is defined to be the temperature at the package pins where contact is made to the circuit board.

## Electrical Specifications $T_c = 25^{\circ}C$ , each diode

PIN General Purpose Diodes, Typical Specifications  $T_A = 25^{\circ}C$ 

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V <sub>BR</sub> (V)	Typical Series Resistance $R_{S}(\Omega)$	Typical Total Capacitance C <sub>T</sub> (pF)
3860 3862 3863 3864 386B 386C 386E 386F 386F 386L	F0 <sup>[1]</sup> F2 <sup>[1]</sup> F3 <sup>[1]</sup> F4 <sup>[1]</sup> L0 <sup>[2]</sup> L2 <sup>[2]</sup> L3 <sup>[2]</sup> L4 <sup>[2]</sup> LL <sup>[2]</sup>	0 2 3 4 B C E F L	Single Series Common Anode Common Cathode Single Series Common Anode Common Cathode Unconnected Trio	50	3.0/1.5*	0.20
Test Conditions				$\begin{array}{l} V_{R}=V_{BR}\\ Measure\\ I_{R}\leq 10 \ \mu A \end{array}$	$\begin{split} I_{\rm F} &= 10 \text{ mA} \\ f &= 100 \text{ MHz} \\ I_{\rm F} &= 100 \text{ mA}^* \end{split}$	V <sub>R</sub> = 50 V f = 1 MHz

#### Notes:

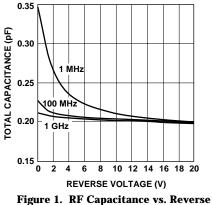
1. Package marking code is white.

2. Package marking code is laser marked.

Part Number HSMP-	Total Resistance R <sub>T</sub> (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T <sub>rr</sub> (ns)	Total Capacitance C <sub>T</sub> (pF)
386x	22	500	80	0.20
Test Conditions	$I_{\rm F} = 1 \text{ mA}$ $f = 100 \text{ MHz}$	$I_{\rm F} = 50 \text{ mA}$ $T_{\rm R} = 250 \text{ mA}$	$\begin{array}{c} V_{R}=10 \ V\\ I_{F}=20 \ mA\\ 90\% \ Recovery \end{array}$	$\begin{array}{l} V_{R}=50 \ V\\ f=1 \ MHz \end{array}$

HSMP-386x Typical Parameters at  $T_C = 25^{\circ}C$ 

**Typical Performance**,  $T_C = 25^{\circ}C$ , each diode



Bias.

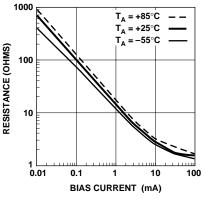


Figure 2. Typical RF Resistance vs. Forward Bias Current.

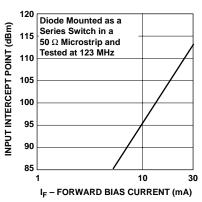


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

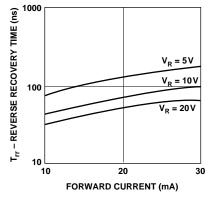
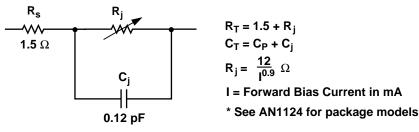
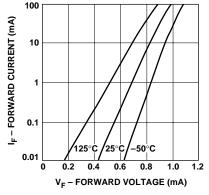
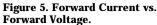


Figure 4. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages.









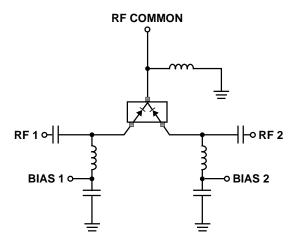


Figure 6. Simple SPDT Switch, Using Only Positive Current.

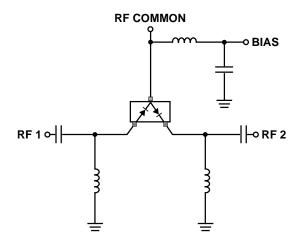


Figure 8. Switch Using Both Positive and Negative Current.

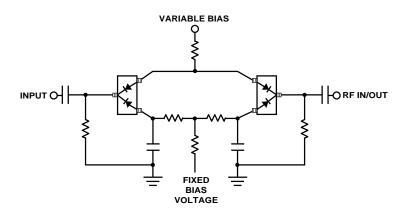


Figure 10. Four Diode  $\pi$  Attenuator. See AN1048 for details.

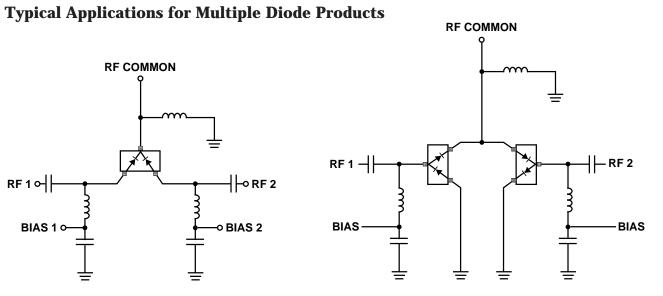


Figure 7. High Isolation SPDT Switch, Dual Bias.

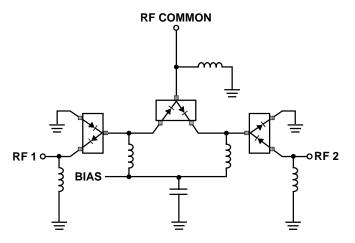
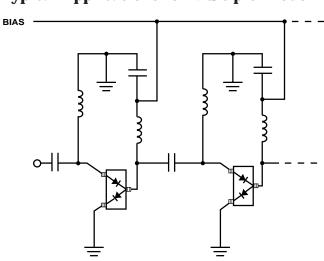


Figure 9. Very High Isolation SPDT Switch, Dual Bias.



# Figure 11. High Isolation SPST Switch (Repeat Cells as Required).

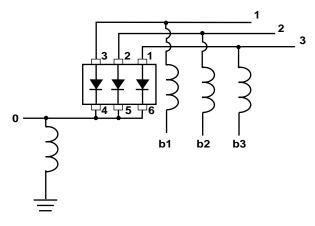
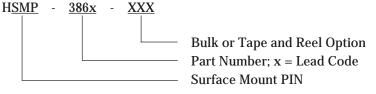


Figure 13. HSMP-386L used in a SP3T Switch.

### **Ordering Information**

Specify part number followed by option. For example:



### **Option Descriptions**

-BLK = Bulk, 100 pcs. per antistatic bag -TR1 = Tape and Reel, 3000 devices per 7" reel -TR2 = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

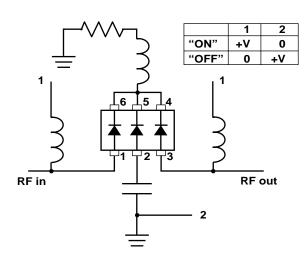


Figure 12. HSMP-386L Unconnected Trio used in a Positive Voltage, High Isolation Switch.

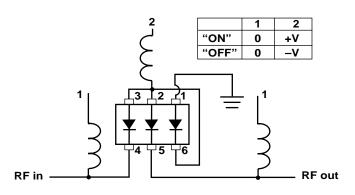


Figure 14. HSMP-386L Unconnected Trio used in a Dual Voltage, High Isolation Switch.

## Typical Applications for Multiple Diode Products (continued)

## Assembly Information

**SOT-323 PCB Footprint** Recommended PCB pad layouts for the miniature SOT packages are shown in Figures 15, 16, 17. These layouts provide ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

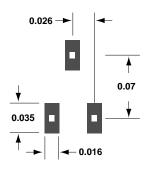


Figure 15. PCB Pad Layout, SOT-323. (dimensions in inches).

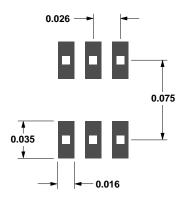
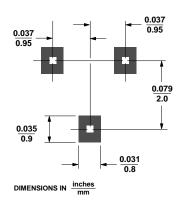


Figure 16. PCB Pad Layout, SOT-363. (dimensions in inches).



#### **SMT Assembly**

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT package, will reach solder reflow temperatures faster than those with a greater mass.

Agilent's diodes have been qualified to the time-temperature profile shown in Figure 18. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cooldown zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone ( $T_{MAX}$ ) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for Agilent diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

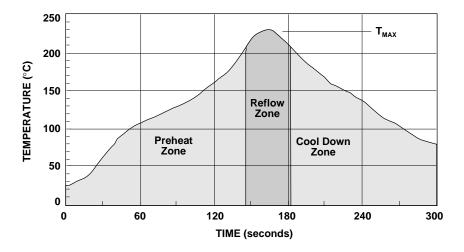
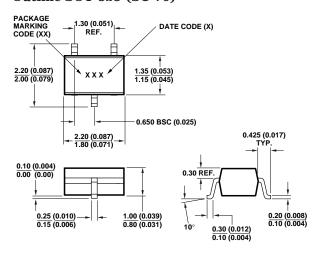


Figure 18. Surface Mount Assembly Profile.

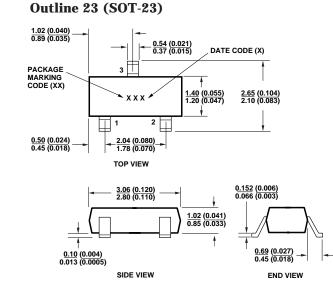
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Figure 17. PCB Pad Layout, SOT-23.

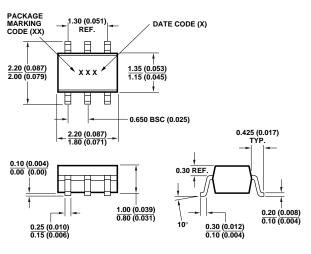
### Package Dimensions Outline SOT-323 (SC-70)



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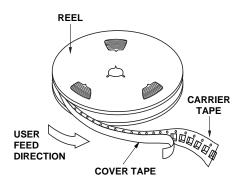
## **Package Characteristics**

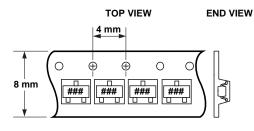
Lead Material Coj	oper (SOT-323/363); Alloy 42 (SOT-23)
Lead Finish	
Maximum Soldering Temperature	
Minimum Lead Strength	
Typical Package Inductance	
	0.08 pF (opposite leads)

### Outline 363 (SC-70, 6 Lead)



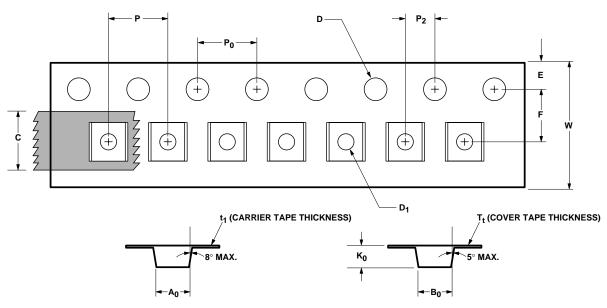
## **Device Orientation**





Note: "###" represents Package Marking Code, Date Code.

## **Tape Dimensions** For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH WIDTH DEPTH PITCH BOTTOM HOLE DIAMETER	A <sub>0</sub> B <sub>0</sub> K <sub>0</sub> P D <sub>1</sub>	$2.24 \pm 0.10 \\ 2.34 \pm 0.10 \\ 1.22 \pm 0.10 \\ 4.00 \pm 0.10 \\ 1.00 + 0.25$	$\begin{array}{c} 0.088 \pm 0.004 \\ 0.092 \pm 0.004 \\ 0.048 \pm 0.004 \\ 0.157 \pm 0.004 \\ 0.039 \pm 0.010 \end{array}$
PERFORATION	FORATION DIAMETER PITCH POSITION		$\begin{array}{c} 1.55 \pm 0.05 \\ 4.00 \pm 0.10 \\ 1.75 \pm 0.10 \end{array}$	$\begin{array}{c} \textbf{0.061} \pm \textbf{0.002} \\ \textbf{0.157} \pm \textbf{0.004} \\ \textbf{0.069} \pm \textbf{0.004} \end{array}$
CARRIER TAPE	WIDTH THICKNESS	W t <sub>1</sub>	$\begin{array}{c} \textbf{8.00} \pm \textbf{0.30} \\ \textbf{0.255} \pm \textbf{0.013} \end{array}$	$\begin{array}{c} \textbf{0.315} \pm \textbf{0.012} \\ \textbf{0.010} \pm \textbf{0.0005} \end{array}$
COVER TAPE	TAPE WIDTH TAPE THICKNESS		$\begin{array}{c} \textbf{5.4} \pm \textbf{0.10} \\ \textbf{0.062} \pm \textbf{0.001} \end{array}$	$\begin{array}{c} \textbf{0.205} \pm \textbf{0.004} \\ \textbf{0.0025} \pm \textbf{0.00004} \end{array}$
DISTANCE CAVITY TO PERFORATION (WIDTH DIRECTION) CAVITY TO PERFORATION (LENGTH DIRECTION)		F P <sub>2</sub>	$\begin{array}{c} \textbf{3.50} \pm \textbf{0.05} \\ \textbf{2.00} \pm \textbf{0.05} \end{array}$	$\begin{array}{c} \textbf{0.138} \pm \textbf{0.002} \\ \textbf{0.079} \pm \textbf{0.002} \end{array}$

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