Agilent Technologies
Innovating the HP Way

3-volt, Low Noise Amplifier for 0.8 – 6 GHz Applications

Technical Data

MGA-85563

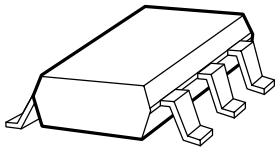
Features

- **1.6 dB minimum Noise Figure at 1.9 GHz**
- **Adjustable IP3 from +12 dBm to +17 dBm via External Resistor**
- **18 dB Gain at 1.9 GHz**
- **Single 3 V Supply**
- **Unconditionally Stable**

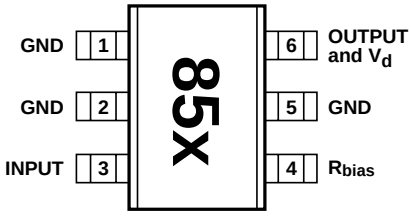
Applications

- **Amplifier for Cellular, PCS, and Wireless LAN Applications**

Surface Mount Package SOT-363 (SC-70)



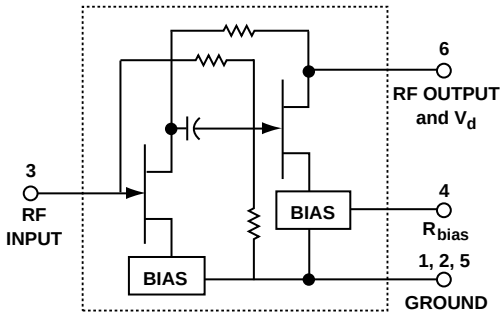
Pin Connections and Package Marking



Note:
Package marking provides orientation and identification; "x" is date code.

Equivalent Circuit

(Simplified)



Description

Agilent's MGA-85563 is an easy-to-use GaAs RFIC amplifier that offers low noise figure and high gain from 0.8 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The MGA-85563 features a minimum noise figure of 1.6 dB and associated gain of 18 dB at 1.9 GHz. The output is matched internally to 50 Ω, and the input is partially matched, requiring only a single external inductor for optimal performance. The supply current can be adjusted using an external resistor, varying IP3 from +12 dBm to +17 dBm.

The circuit uses state-of-the-art PHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3 V supply, while resistive feedback ensures stability (K > 1) over frequency and temperature.

MGA-85563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d, max	Maximum Device Voltage	V	5.5
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{ch\ to\ c} = 155°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $Z_O = 50\ \Omega$, $V_d = 3$ V, and using default of no external resistor at the R_{bias} pin

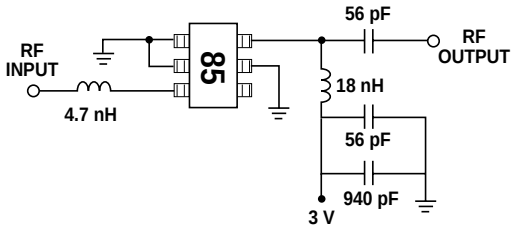
Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std. Dev.[3]
G_{test}	Gain in Test Circuit[1]	f = 2.0 GHz	dB	16	19		1.0
NF_{test}	Noise Figure in Test Circuit[1]	f = 2.0 GHz	dB		1.85	2.3	0.1
NF_{MIN}	Minimum Noise Figure	f = 0.9 GHz	dB		1.6		
	(measured with Γ_{opt} presented to the	f = 1.5 GHz			1.6		
	input and 50 Ω presented to the output)	f = 2.0 GHz			1.6		0.1
		f = 2.4 GHz			1.6		
		f = 4.0 GHz			1.6		
		f = 5.0 GHz			1.6		
		f = 6.0 GHz			1.6		
G_A	Associated Gain at NF_{MIN}	f = 0.9 GHz	dB		17.0		
	(measured with Γ_{opt} presented to the	f = 1.5 GHz			17.5		
	input and 50 Ω presented to the output)	f = 2.0 GHz			18.0		1.0
		f = 2.4 GHz			18.5		
		f = 4.0 GHz			17.5		
		f = 5.0 GHz			16.0		
		f = 6.0 GHz			14.5		
IP_3	Third Order Intercept Point	f = 0.9 GHz	dBm		13		
	(measured with 50 Ω presented	f = 1.5 GHz			13		
	to the input and output)	f = 2.0 GHz			11.5		1.2
		f = 2.4 GHz			11.5		
		f = 4.0 GHz			13		
		f = 5.0 GHz			12.5		
		f = 6.0 GHz			12		
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.9 GHz	dBm		0.8		
	(measured with 50 Ω presented	f = 1.5 GHz			0.9		
	to the input and output)	f = 2.0 GHz			0.9		1.1
		f = 2.4 GHz			1.0		
		f = 4.0 GHz			1.4		
		f = 5.0 GHz			1.3		
		f = 6.0 GHz			1.2		

MGA-85563 Electrical Specifications, continued, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, and using default of no external resistor at the R_{bias} pin

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.	Std. Dev.[3]
$VSWR_{in}$	Input VSWR[2]			2.5:1		
$VSWR_{out}$	Output VSWR[2]			1.3:1		
ISOL	Isolation f = 0.9 – 3.0 GHz f = 3.0 – 6.0 GHz	dB		37 30		0.6
I_d	Device Current	mA		15	20	1.9

Notes:
1. Guaranteed specifications are 100% tested in the circuit of Figure 1.
2. Measured using the final test circuit shown below at f = 2 GHz.
3. Standard Deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

MGA-85563 Final Test Circuit, T_C = 25°C, Z_O = 50 Ω



MGA-85563 Typical Performance, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, and using default of no external resistor at the R_{bias} pin

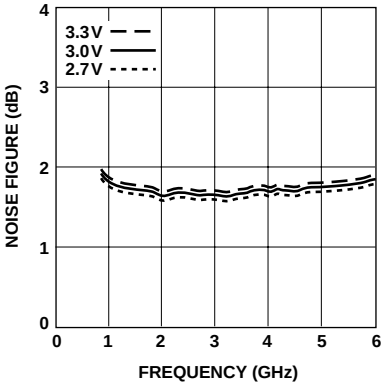


Figure 1. Minimum Noise Figure vs. Frequency and Voltage.

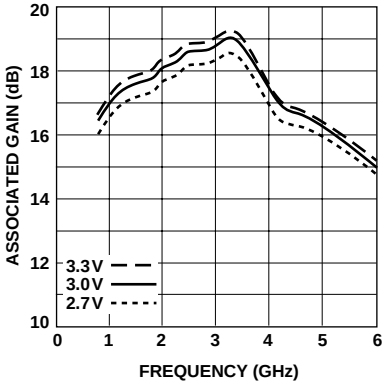


Figure 2. Associated Gain vs. Frequency and Voltage.

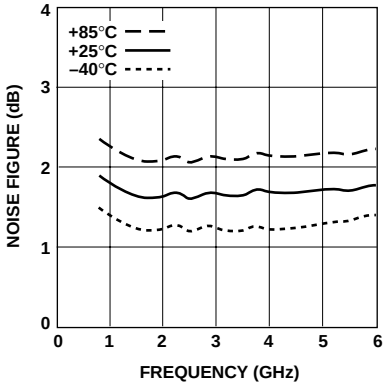


Figure 3. Minimum Noise Figure vs. Frequency and Temperature.

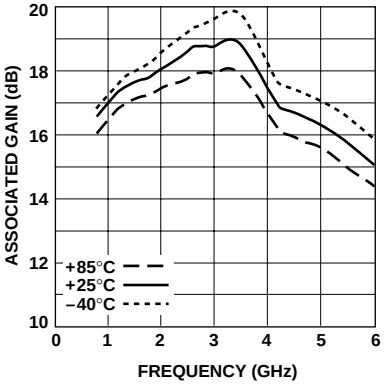


Figure 4. Associated Gain vs. Frequency and Temperature.

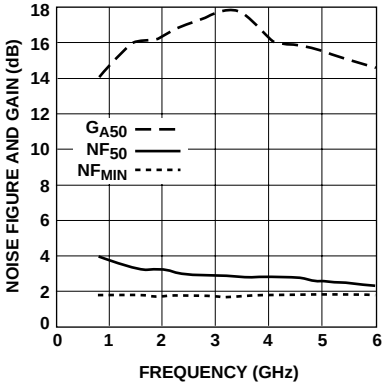


Figure 5. Gain and Noise Figure (50 Ω Source and Load) vs. Frequency.

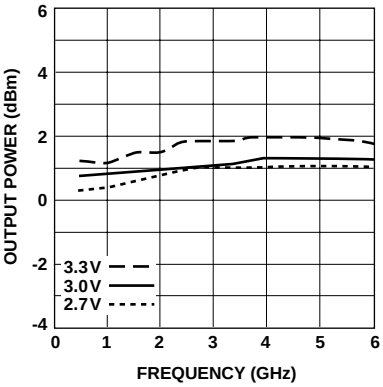


Figure 6. Output Power @ 1 dB Gain Compression vs. Frequency and Voltage.

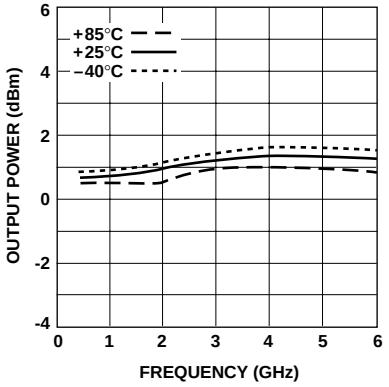


Figure 7. Output Power @ 1 dB Gain Compression vs. Frequency and Temperature.

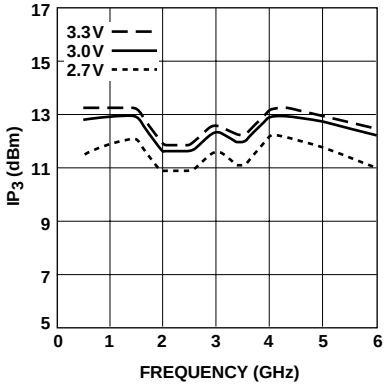


Figure 8. Output Third Order Intercept Point vs. Frequency and Voltage.

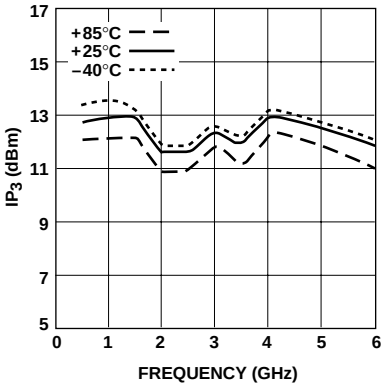


Figure 9. Output Third Order Intercept Point vs. Frequency and Temperature.

MGA-85563 Typical Performance, continued, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, and using default of no external resistor at the R_{bias} pin

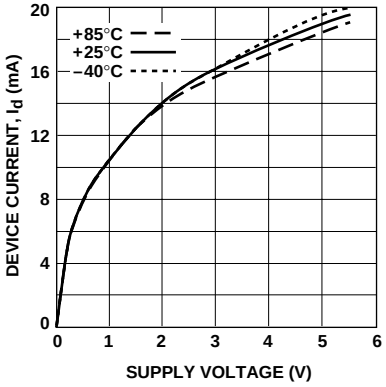


Figure 10. Device Current vs. Voltage and Temperature.

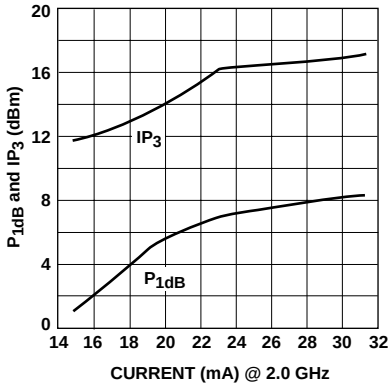


Figure 11. Output Third Order Intercept and P_{1dB} vs. Device Current.

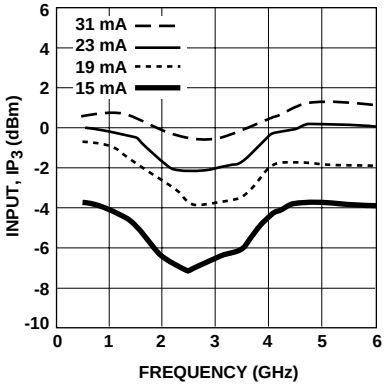


Figure 12. Input Third Order Intercept vs. Frequency and Device Current.

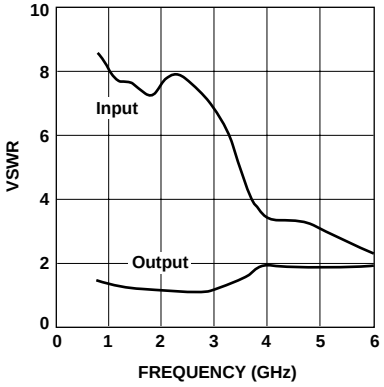


Figure 13. Input and Output VSWR vs. Frequency.

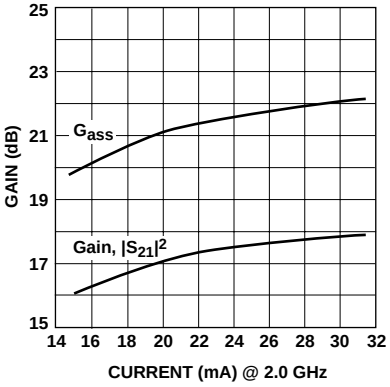


Figure 14. Gain, $|S_{21}|^2$, and Gain Associated with Minimum Noise vs. Current.

MGA-85563 Typical Scattering Parameters, T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, and using default of no external resistor at the R_{bias} pin

Freq.	S_{11}			S_{21}			S_{12}			S_{22}			K
GHz	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Factor
0.2	-1.1	0.88	-10	4.0	1.6	115	-30.8	0.029	1	-4.5	0.60	-42	2.1
0.5	-1.7	0.82	-15	11.5	3.8	66	-33.6	0.021	-18	-9.8	0.32	-69	2.1
0.9	-2.1	0.79	-22	14.8	5.5	27	-35.9	0.016	-16	-15.3	0.17	-79	2.3
1.0	-2.2	0.78	-24	15.2	5.7	20	-36.5	0.015	-15	-16.2	0.16	-78	2.3
1.5	-2.2	0.77	-34	16.4	6.6	-11	-39.2	0.011	-8	-19.3	0.11	-81	2.7
1.8	-2.3	0.76	-39	16.5	6.7	-26	-41.1	0.009	5	-19.5	0.11	-88	3.5
1.9	-2.3	0.77	-41	16.6	6.7	-30	-41.3	0.009	16	-19.7	0.10	-97	3.6
2.0	-2.3	0.77	-43	16.6	6.8	-34	-41.0	0.009	26	-20.5	0.09	-110	3.4
2.1	-2.2	0.77	-45	16.8	6.9	-38	-40.3	0.010	31	-22.0	0.08	-123	3.1
2.2	-2.2	0.78	-48	16.9	7.0	-42	-39.2	0.011	34	-24.2	0.06	-136	2.8
2.3	-2.2	0.78	-50	17.1	7.0	-47	-39.2	0.011	37	-25.8	0.05	-149	2.6
2.4	-2.2	0.77	-53	17.2	7.2	-51	-39.2	0.011	39	-27.1	0.04	-164	2.5
2.5	-2.3	0.77	-55	17.3	7.3	-55	-38.4	0.012	42	-28.2	0.04	176	2.4
3.0	-2.6	0.75	-68	17.6	7.6	-78	-35.9	0.016	57	-22.4	0.08	113	1.8
3.5	-3.4	0.68	-84	17.8	7.7	-102	-31.7	0.026	61	-15.0	0.18	92	1.3
4.0	-5.4	0.54	-90	16.3	6.5	-126	-28.9	0.036	38	-10.2	0.31	51	1.4
4.5	-5.3	0.55	-96	15.7	6.1	-139	-30.2	0.031	27	-11.1	0.28	26	1.7
5.0	-5.9	0.51	-110	15.4	5.9	-156	-29.9	0.032	29	-11.1	0.28	15	1.8
5.5	-6.8	0.46	-123	15.0	5.6	-173	-29.6	0.033	26	-11.1	0.28	4	1.9
6.0	-8.2	0.39	-136	14.4	5.3	169	-28.9	0.036	25	-10.8	0.29	-7	2.0
6.5	-9.4	0.34	-150	13.8	4.9	152	-28.0	0.040	23	-10.5	0.30	-17	2.1
7.0	-10.8	0.29	-164	13.0	4.5	136	-27.1	0.044	19	-10.1	0.31	-26	2.1
7.5	-12.3	0.24	-174	12.1	4.0	120	-26.2	0.049	14	-9.8	0.33	-35	2.2
8.0	-13.5	0.21	172	11.3	3.7	106	-25.7	0.052	8	-9.4	0.34	-45	2.2

MGA-85563 Typical Noise Parameters,

T_C = 25°C, Z_O = 50 Ω, V_d = 3 V, and using default of no external resistor at the R_{bias} pin

Frequency	F_{min}	Γ_{opt}		R_N
(GHz)	(dB)	Mag.	Ang.	(Ω)
0.2	1.63	0.70	28	0.86
0.5	1.61	0.67	29	0.81
0.9	1.60	0.63	29	0.73
1.0	1.59	0.62	29	0.72
1.5	1.57	0.57	30	0.63
1.8	1.56	0.56	32	0.59
1.9	1.56	0.56	33	0.59
2.0	1.56	0.56	34	0.58
2.1	1.56	0.56	35	0.57
2.2	1.56	0.55	37	0.55
2.3	1.56	0.54	39	0.53
2.4	1.56	0.54	41	0.52
2.5	1.56	0.53	42	0.51
3.0	1.57	0.50	49	0.47
3.5	1.56	0.49	54	0.43
4.0	1.57	0.49	61	0.41
4.5	1.58	0.46	69	0.37
5.0	1.59	0.43	78	0.32
5.5	1.59	0.40	86	0.29
6.0	1.63	0.35	94	0.25
6.5	1.65	0.25	104	0.23
7.0	1.66	0.15	114	0.20
7.5	1.68	0.06	125	0.18
8.0	1.70	0.04	-48	0.15

MGA-85563 Applications Information

Description

The MGA-85563 is a two-stage, low noise GaAs RFIC amplifier designed for receiver applications in the 800 MHz to 5.8 GHz frequency range. The device combines low noise performance with high linearity to make it a desirable choice for receiver front end stages.

A special feature of the MGA-85563 is the ability to customize its output power capability for higher linearity by setting the device's current. For applications requiring additional dynamic range, the third order intercept point can be boosted by up to 6 dB by using this feature.

The MGA-85563 operates from a +3-volt power supply and draws a nominal current of 15 mA. The RFIC is contained in a miniature SOT-363 (SC-70) package to minimize printed circuit board space. The combination of 3-volt operation and small size are important to designers of miniature, battery-powered wireless communications products such as cellular telephones, PCS, and RF modems.

The high frequency response of the MGA-85563 extends through 6 GHz making it an excellent choice for use in 5 GHz RLL as well as 2.4 and 5.7 GHz spread spectrum and ISM/license-free band applications.

Internal, on-chip capacitors limit the low end frequency response to applications above approximately 500 MHz.

Application Guidelines

The MGA-85563 is very easy to use. For most applications, all that is required to operate the MGA-85563 is to apply +3 volts to the RF Output pin, and noise match the RF Input.

RF Input

To achieve lowest noise figure performance, the input of the MGA-85563 should be matched from the system impedance (typically 50 Ω) to the optimum source impedance for minimum noise, Γ_{opt}. Since the real part of the input of the device impedance is near 50 Ω and the reactive part is capacitive, a simple series inductor at the input is often all that is needed to provide a suitable noise match for many applications.

RF Output

The RF Output port is internally matched to 50 Ω and will not normally require additional matching.

DC Bias

DC bias is applied to the MGA-85563 through the RF Output connection. Figure 15 shows how an inductor (RFC) is used to isolate the RF signal from the DC supply. The bias line is capacitively bypassed to keep RF from the DC supply lines and prevent resonant dips or peaks in the response of the amplifier.

The DC schematic for an MGA-85563 amplifier circuit is shown in Figure 15.

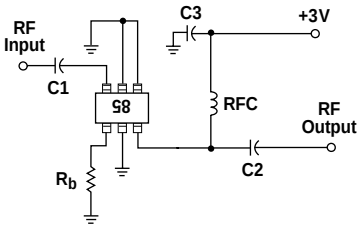


Figure 15. Schematic Diagram with Bias and Current Setting Connections.

A DC blocking capacitor (C2) is used at the output of the RFIC to isolate the supply voltage from succeeding circuits.

While the RF input terminal of the MGA-85563 is at DC ground potential, it should not be used as a current sink. If the input is connected directly to a preceding stage that has a DC voltage present, a blocking capacitor (C1) should be used.

Setting the Bias Current for Higher Linearity

The MGA-85563 has a feature that allows the user to place an external resistor (R_b) from the R_{bias} pin to DC ground and thereby increase the device current. The current can be raised from its nominal 15 mA up to approximately 50 mA. The higher current increases amplifier linearity by boosting output power (P_{1dB}) by up to 8 dB. Maximum linearity performance is obtained at a current of 30 to 35 mA. Currents greater than 35 mA are not recommended since the output power has reached a point of diminishing returns at this current.

Figure 16 shows the relationship between device current and the value of the external resistor.

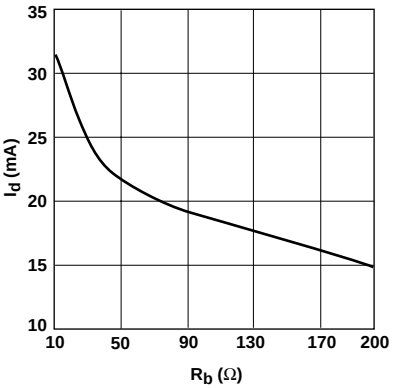


Figure 16. Bias Current vs. Resistor Value.

The current is increased only in the second stage of the MGA-85563. Bias current for the first stage remains fixed and thus the input impedance and noise figure for the amplifier are unaffected by the increase in bias current. The output match is also generally unaffected by increased device current and remains quite good over the complete operating current and frequency range.

PCB Layout

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package that is used by the MGA-85563 is shown in Figure 17.

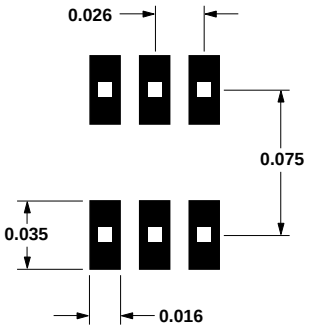


Figure 17. PCB Pad Layout for MGA-85563 Package (dimensions in inches).

This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-85563. The layout is shown with a footprint of a SOT-363 package superimposed on the PCB pads for reference.

Starting with the package pad layout in Figure 17, an RF layout similar to the one shown in Figure 18 a good starting point for microstripline designs using the MGA-85563 amplifier.

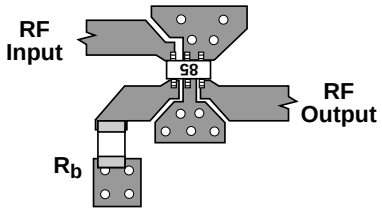


Figure 18. RF Layout.

Adequate grounding of Pins 1, 2, and 5 of the RFIC are important to maintain device stability and RF performance. Each of the ground pins should be connected to the groundplane on the backside of the PCB by means of plated through holes (vias). The ground vias should be placed as close to the package terminals as practical. At least one via should be located next to each ground pin to assure good RF grounding. It is a good practice to use multiple vias to further minimize ground path inductance.

If the adjustable current feature is to be used, an additional ground pad located near the R_{bias} pin may be used to connect the current-setting resistor (R_b) directly from the R_{bias} pin to ground. (The ground pad for Pin 5 could also be used for this purpose.) Note that when using an external resistor, the R_{bias} pad *should not* be bypassed to ground. Doing so could result in undesirable resonances in the amplifier gain response.

If for any reason the R_b resistor is not located immediately adjacent to the MGA-85563 (such as in the case of remote current adjustment or to implement dynamic control of the device's linearity), then a small series resistor (e.g., 10 Ω) should be located near the R_{bias} pin to de-Q the connection from the MGA-85563 to the external current-setting circuit.

If the adjustable current feature of the MGA-85563 is not used, the R_{bias} pin should be left open. When not used, the PCB pad for the R_{bias} pin should only be large enough to provide a mechanical attachment, such as shown in Figure 17. If a large pad or length of line is connected to the R_{bias} pad, a potential exists for the pad parasitics to interact with the internal circuitry of the MGA-85563 to create an undesirable resonance in the gain response of the amplifier.

While it might be considered an effective RF practice, it is recommended that the PCB pads for the ground pins *not* be connected together underneath the body of the package. In many cases, it is important that the individual stages within the device be grounded separately to prevent inadvertent interstage feedback. In addition, PCB traces hidden under the package cannot be adequately inspected for SMT solder bridging or quality.

PCB Materials

FR-4 or G-10 type materials are good choices for most low cost wireless applications using single or multi-layer printed circuit boards. Typical single-layer board thickness is 0.020 to 0.031 inches. Circuit boards thicker than 0.031 inches are not recom-

mended due to excessive inductance in the ground vias.

For noise figure critical or higher frequency applications, the additional cost of PTFE/glass dielectric materials may be warranted to minimize transmission line loss at the amplifier's input.

Application Example

The printed circuit layout in Figure 19 can be used with the MGA-85563 for frequencies from 800 MHz through 6 GHz. This layout is a microstripline design (solid groundplane on the backside of the circuit board) with 50 Ω interfaces for the RF input and output. The circuit is fabricated on 0.031-inch thick FR-4 dielectric material. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the paths to ground.

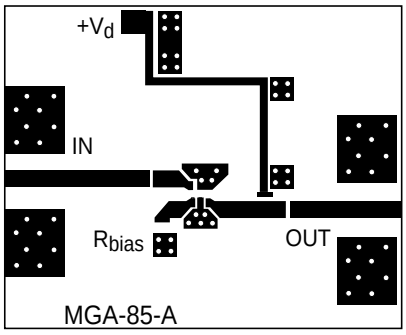


Figure 19. Multi-purpose PCB Layout.

1.9 GHz Design

To illustrate the simplicity of using the MGA-85563, a 1.9 GHz amplifier for PCS type receiver applications is presented.

To achieve minimum noise figure, the 50 Ω input to the amplifier is matched to Γ_{opt}. From the table of Typical Noise Parameters, the value of Γ_{opt} at 1.9 GHz is found to be 0.56 ∠+33°. The conjugate of Γ_{opt}, 0.56 ∠-33°, is plotted on the Smith chart as Point A in Figure 20. The addition of a 0.108 inch length (actual length on FR-4; electrical length is 11.7° of 50 Ω transmission line (MLIN) rotates Point A around to the R = 1 circle on the Smith chart. A series 5.6 nH inductor (L1) is then all that is required to complete the match to 50 Ω.

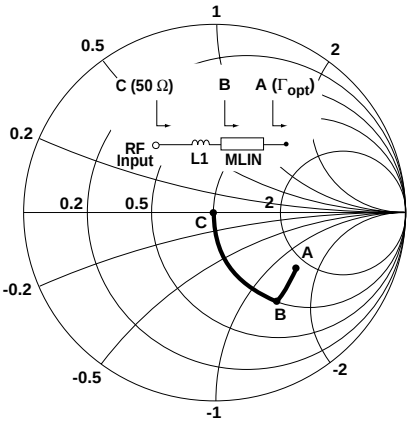


Figure 20. Input Impedance Match.

The output of the MGA-85563 is already well matched to 50 Ω and no additional matching is needed.

The resulting RF circuit is shown in Figure 21.

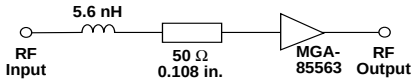


Figure 21. Input Circuit for 1.9 GHz.

A schematic diagram of the complete 1.9 GHz circuit with the input noise match and DC biasing is shown in Figure 22.

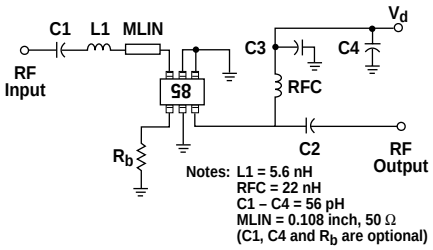


Figure 22. Schematic of 1.9 GHz Circuit.

DC bias is applied to the MGA-85563 through the RFC at the RF Output pin. The power supply connection is bypassed to ground with capacitor C3. Provision is made for an additional bypass capacitor, C4, to be added to the bias line near the +3 volt connection. C4 will not normally be needed unless several stages are cascaded using a common power supply.

The optional resistor, R_b, may be added if desired to increase device current to handle higher level signals. The use of the bias-setting resistor will not affect the input matching circuit.

Since the input terminal of the MGA-85563 is at ground potential, the input DC blocking capacitor C1 need not be used unless the amplifier is connected to a preceding stage that has a voltage present at this point.

The value of the DC blocking and RF bypass capacitors (C1 – C4) should be chosen to provide a small reactance (typically <2 ohms) at the lowest operating frequency. For this 1.9 GHz design example, 56 pF capacitors with a reactance of 1.5 ohms are adequate. The reactance of the RF choke (RFC) should be high (i.e., several hundred ohms) at

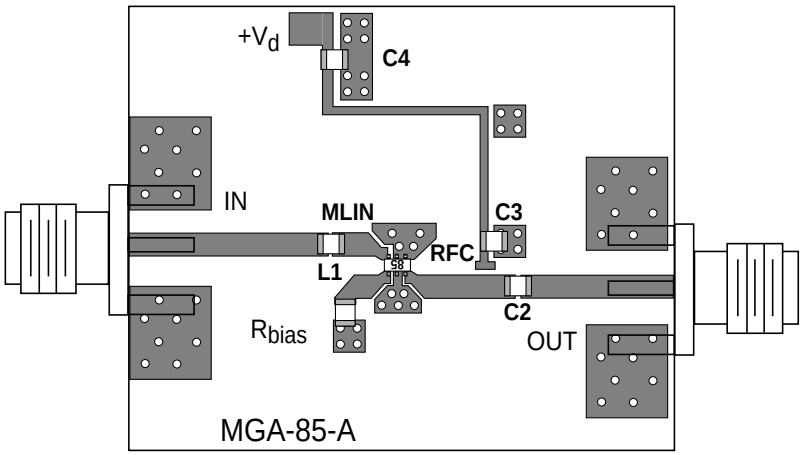


Figure 23. Complete 1.9 GHz Amplifier Circuit.

the lowest frequency of operation. A 22 nH inductor with a reactance of 262 ohms at 1.9 GHz is sufficiently high to minimize the loss from circuit loading.

The completed 1.9 GHz amplifier for this example with all components and SMA connectors assembled is shown in Figure 23.

Designs for Other Frequencies

The same basic design approach described above for 1.9 GHz can be applied to other frequency bands. Inductor values for matching the input for low noise figure are shown in Table 1.

For frequencies below 1000 MHz, the series input inductor approach provides a good match but may not completely noise match the MGA-85563. A two-element matching circuit may be required at lower frequencies to exactly match the input to Γ_{opt}. At lower frequencies, the real part of Γ_{opt} has started to move away from 50 Ω (i.e., away from the R = 1 circle on the Smith chart) as the angle of Γ_{opt} decreases. A small shunt capacitor (typically 0.4 to 0.9 pF) added between the input pin and the adjacent ground pad to create a shunt C-series L matching network will realize an improvement in noise figure of several tenths of a dB. A lower value for L1 may be needed depending on the actual length of the input line between Pin 1 and L1 as well as the value of the shunt C.

For frequencies above 3 GHz, the input is already well matched to 50 Ω and no additional matching is normally needed.

Frequency (GHz)	L1 (nH)
0.8*	22
0.9*	18
1.5	8.2
1.9	5.6
2.4	2.7
5.1	0
5.8	0

Table 1. Input Inductor Values for Various Operating Frequencies. (*Additional matching required for optimum NF).

Actual component values may differ slightly from those shown in Table 1 due to variations in circuit layout, grounding, and component parasitics. A CAD program such as Agilent's *Touchstone*® is recommended to fully analyze and account for these circuit variables.

Hints and Troubleshooting

Oscillation

Unconditional stability of the MGA-85563 is dependent on having very good grounding. Inadequate device grounding or poor PCB layout techniques could cause the device to be potentially unstable.

Even though a design may be unconditionally stable (K > 1 and B1 > 0) over its full frequency range, other possibilities exist that may cause an amplifier circuit to oscillate. One thing to check is feedback in bias circuits. It is important to capacitively bypass the connections to active bias circuits to ensure stable operation. In multistage circuits, feedback through bias lines can also lead to oscillation.

Components of insufficient quality for the frequency range of the amplifier can sometimes lead to instability. Also, component values that are chosen to be much higher in value than is appropriate for the application can present a problem. In both of these cases, the components may have reactive parasitics that make their impedances very different than expected. Chip capacitors may have excessive inductance, or chip inductors can exhibit resonances at unexpected frequencies.

A Note on Supply Line Bypassing

Multiple bypass capacitors are normally used throughout the power distribution within a wireless system. Consideration should be given to potential resonances formed by the combination of these capacitors and the inductance of the DC distribution lines. The addition of a small value resistor in the bias supply line between bypass capacitors will often de-Q the bias circuit and eliminate resonance effects.

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from three non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard bell curve.

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the MGA-85563, these parameters are: Gain (G_{test}), Noise Figure (NF_{test}), and Device Current (I_d). Each of the guaranteed parameters is 100% tested as part of the manufacturing process.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the center of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate amplifier circuit using the MGA-85563, but to also evaluate and optimize trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 24 for example, the probability of a parameter being between ±1σ is 68.3%; between ±2σ is 95.4%; and between ±3σ is 99.7%.

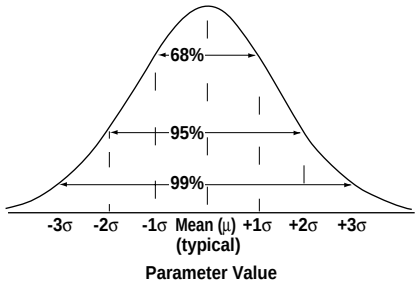


Figure 24. Normal Distribution.

Phase Reference Planes

The positions of the reference planes used to specify S-parameters and Noise Parameters for the MGA-85563 are shown in Figure 25. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

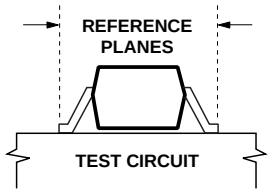


Figure 25. Phase Reference Planes.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The MGA-85563 is qualified to the time-temperature profile shown in Figure 26. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evapo-

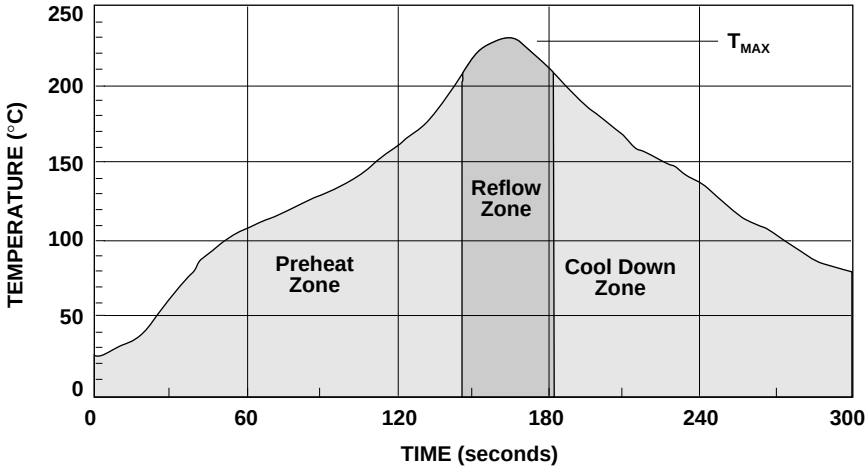


Figure 26. Surface Mount Assembly Profile.

rating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for the MGA-85563. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the MGA-85563 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance, reliability, or failure.

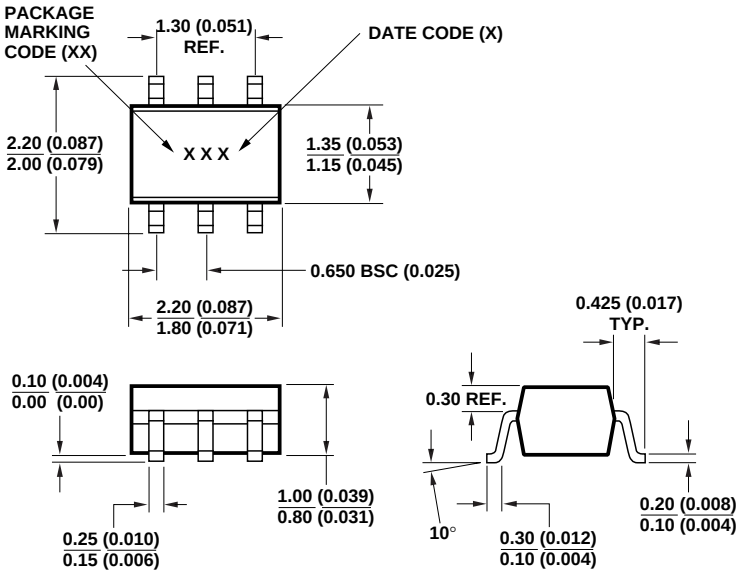
Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage & handling
- Inspection & testing
- Assembly
- In-circuit use

The MGA-85563 is a ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

Package Dimensions

Outline 63 (SOT-363/SC-70)

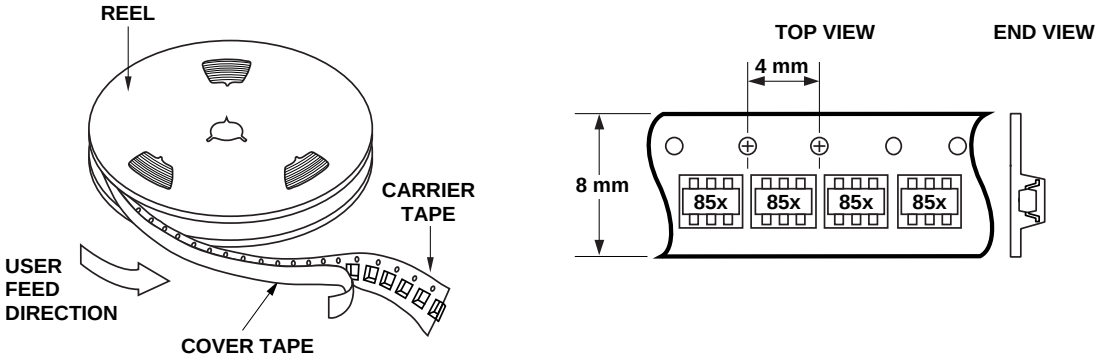


DIMENSIONS ARE IN MILLIMETERS (INCHES)

MGA-85563 Part Number Ordering Information

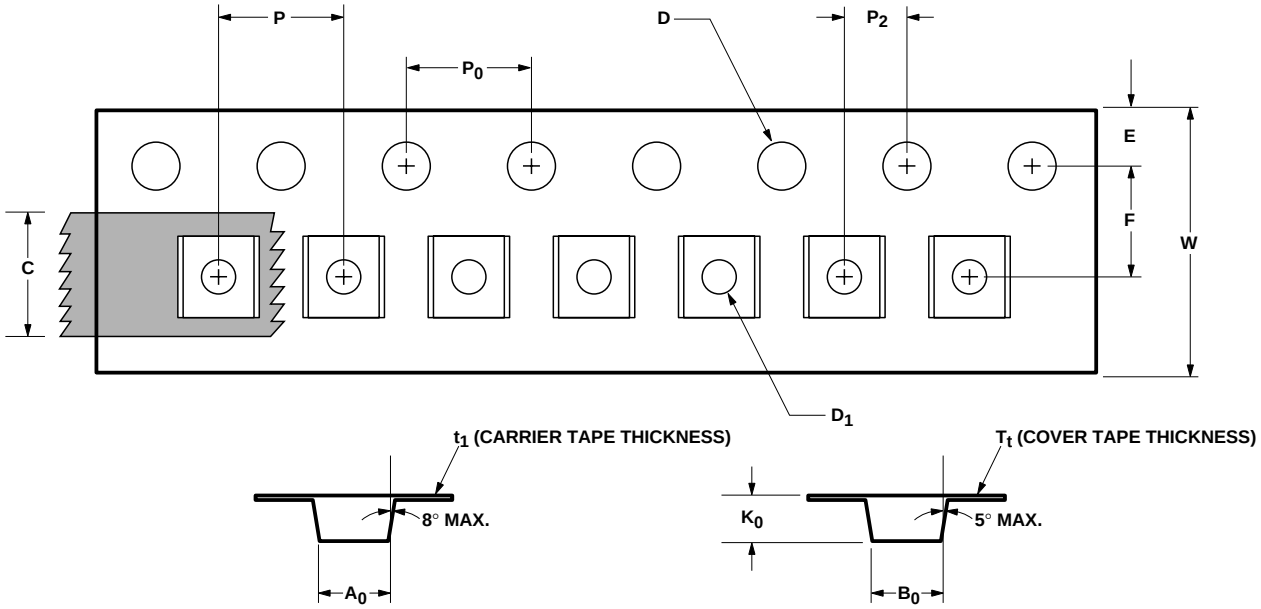
Part Number	Devices per Container	Container
MGA-85563-TR1	3000	7" reel
MGA-85563-BLK	100	Antistatic bag

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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Data subject to change.

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