MC33170

RF Amplifier Companion Chip for Dual-Band Cellular Subscriber Terminal

The MC33170 is a complete solution for drain modulated dual–band GSM 900MHz and DCS–1800MHz Power Amplifiers. Thanks to its internal decoder, the MC33170 drastically simplifies the interface between the PAs and the baseband logic section, providing an immediate gain in part count but also in occupied copper area. The device is also ready for 1V platforms since it accepts logic high control signals down to 900mV@25°C.

A priority management system ensures the negative is present before authorizing the power modulation, giving the necessary ruggedness to the final design. This function can easily be disabled for PAs not requiring a negative bias.

The device is able to directly drive an external P or N–channel with the possibility to linearize the overall response via the internal high–performance control amplifier and easily implement system gain.

Finally, an LDO delivers a stable voltage, usable for external biasing purposes.

- 1V platform compatible: ON voltage = 900mV, OFF voltage = 300mV max
- Priority management system prevents power modulation before negative bias establishes
- High performance 4.5MHz gain–bandwidth product operational amplifier
- Drives N or P–channel MOSFET
- 2.5V low–noise LDO
- Idle mode input for very low power consumption (standby mode)

ON Semiconductor™

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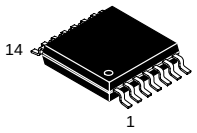
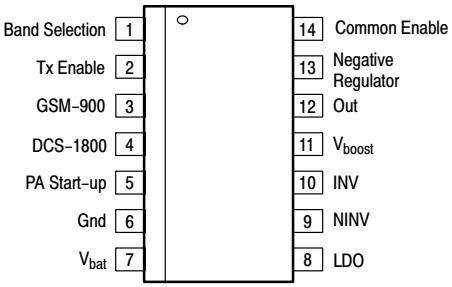


TSSOP–14
DTB SUFFIX
CASE 948G

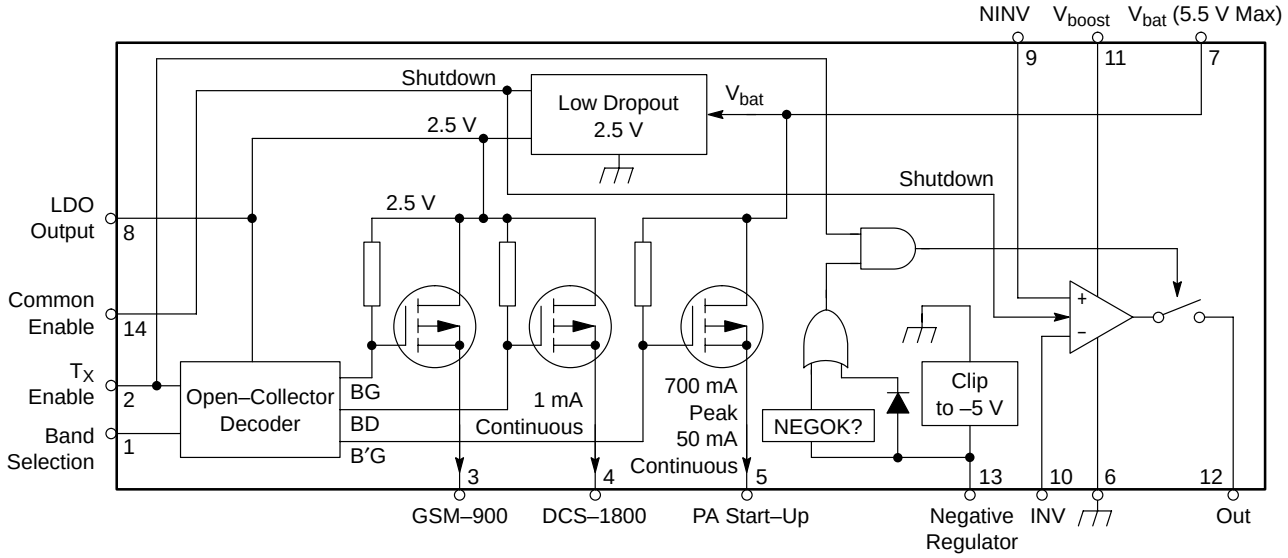
PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33170DTB	TSSOP–14	96 Units / Rail
MC33170DTBR2	TSSOP–14	2500 / Tape & Reel



PIN DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Band Selection	Selects the transmit band	A level high on this input selects the DCS chain. A zero selects the GSM chain.
2	Tx Enable	Starts the power	A level high on this pin enables the DCS/GSM chain and establishes a low–resistance link between pin 5 and 7
3	GSM–900	Biases the 900MHz section	When pin 1 is at zero and pin 2 goes high, the LDO voltage appears on this pin (pin 14 is high)
4	DCS–1800	Biases the 1.8GHz section	When pin 1 is at one and pin 2 goes high, the LDO voltage appears on this pin (pin 14 is high)
5	PA Start–up	Enables the PA power section	When pin 2 goes high, the battery voltage appears on this pin with a 700mA peak current capability (pin 14 is high)
6	Gnd	The IC ground	The IC ground
7	Vbat	The IC power supply	This pin is wired to the battery terminal. A 100nF decoupling capacitor is recommended, depending on the supply impedance
8	LDO	Low DropOut regulator	This output requires a 100nF decoupling and is able to deliver up to 10mA continuous
9	NINV	Positive OPAMP input	The non–inverting OPAMP input
10	INV	Negative OPAMP input	The inverting OPAMP input
11	Vboost	Boost voltage from the PA	This pin connects to a boost voltage delivered by the RF PA. This boost is necessary when driving an N–channel
12	Out	The OPAMP output	The output of the OPAMP/MOSFET driver pin
13	Negative Reg.	The PA negative clip	This pin clips the PA negative bias to —5V and prevents/authorizes the modulation depending on its typical level : <5.5V —— 2.5V> OK <1.3V —— –3.5V> NOTOK <–4.2V —— –5V> OK Max. clipping current is 5mA
14	Common Enable	Enables the whole IC	When high, this pin puts the IC in on–mode

MAXIMUM RATINGS

Rating	Pin No.	Symbol	Value MIN	Value MAX	Units
Band selection	1	Vband	0	5.5	V
Tx Enable	2	TxEn	0	5.5	V
GSM–900	3	VGSM	–5	5.5	V
DCS–1800	4	VDCS	–5	5.5	V
PA Start–up	5	Vstartup	0	5.5	V
Vbat	7	Vbat	0	5.5	V
NINV	9	V+	0	5.5	V
INV	10	V–	0	5.5	V
Boost voltage	11	Vboost	0	12	V
Negative regulation pin	13	VZ	–5.4	5.5	V
Common Enable	14	CE	0	5.5	V
ESD capability, HBM model	All pins			2	kV
ESD capability, Machine model	All pins			200	V
Steering Switch, continuous output current Steering Switch, continuous output current Steering Switch, peak output current < 1μs	3–4 5 5	GSM/DCS PA startup PA startup		1 50 700	mA mA mA
Maximum power dissipation NW suffix, plastic package @Tj=25°C NW suffix, plastic package @Tj=85°C Thermal resistance Junction–to–Air		PD PD RJ–A		500 200 200	mW mW °C/W
Operating Ambient Temperature Maximum Junction Temperature Maximum Operating Junction Temperature		TA Tjmax Tj		–40 to +85 150 125	°C °C °C
Storage Temperature Range		TSTG		–60 to +150	°C

Note1: The control pins, CE, TxEn and Bands shall never exceed Vcc + 0.3V
Note2: A 100nF decoupling capacitor is recommended between the IC Vcc and ground
Note3: To avoid any damage to the IC, the following sequence must be secured:
CE goes up then Tx goes up ——> modulation startup
TX goes down then CE goes down ——> modulation stop

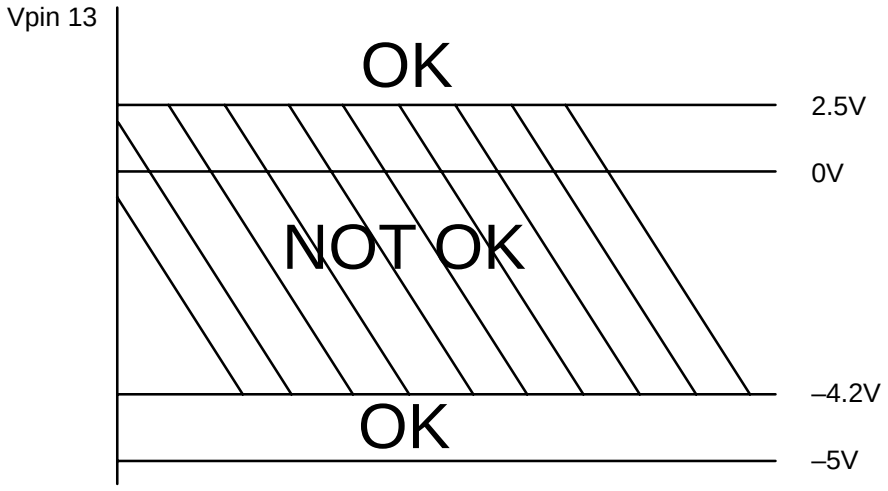
ELECTRICAL CHARACTERISTICS

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
INPUT SPECIFICATIONS						
(For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
Input voltage range	7	V_{bat}	2.7	3.6	5.5	V
Quiescent Current (ON mode) 1 band operating, no load, Vneg. Reg.= –4.2V, V_{CE} = 900mV		I_{QON}		1.0	3.0	mA
Standby current (OFF mode) CE pin at low level, V_{bat} = 5.5V, V_{NEG} and V_{boost} open		I_{QOFF}		1.0	10	μA
LOGIC CONTROL SPECIFICATIONS						
Logic Levels (For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
Logic Level zero Band Selection, Common Enable, TxEn	1–2 14	OFF			300	mV
Logic Level one Band Selection, Common Enable, TxEn	1–2 14	ON	900			mV
Timings (T_A = 25°C)						
Transmission Enable, device already ON 10% of TxEn to 90% of Vbat on PA start–up pin					4.0	μs
VOLTAGE REGULATOR SPECIFICATIONS						
Option section (For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
Output voltage	8	VregOUT	2.45	2.5	2.55	V
Output current	8	IregOUT			10	mA
Short circuit current (Vout = Vnominal – 300mV)	8	$Ireg_{SHORT}$	20			mA
Line regulation Vin = Vout + 1V to 5.5V, device is ON 10mA load on pin 8, 100nF	7–8			400		μV
Dropout voltage at Iout = 10mA	8	VregDROP			150	mV
Output capacitor	8	CregOUT			100	nF
Dynamic parameters (T_A = 25°C)						
Ripple rejection F = 1kHz, Vin = Vout + 1V, Iout = 1mA, Cout = 100nF	8	PSRR		–70		dB
RMS Noise voltage Iout = 1mA, Cout = 100nF, <20Hz — 200kHz>	8			100		μV
Noise density @ 1kHz Iout = 1mA, Cout = 100nF	8	e_n		330		nV/Hz
Rise time : 10% of CE to 90% of $Vreg_{OUT}$	14–8			5.0		μs
CONTROL AMPLIFIER SPECIFICATIONS						
(For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
Continuous current	12	I_{CONT}			2.0	mA
Peak current (sink and source)	12	I_{PEAK}			10	mA
Quiescent current entering pin 11 at 8V Device is in ON state and no load on pin 12	12	I_{QON}		1.0		mA
Input bias current, V+ = V– = 2V		I_{IB}		600		nA
Open–loop voltage gain, TA = 25°C		A_{VOL}		60		dB
Gain Bandwidth Product measured at 100kHz		GBW		5.5		MHz
Output voltage levels, Vnegreg=–5V Level high : Isource = 1mA Level low : Isink = 1mA	12	 V_{OH} V_{OL}	 7.75		 0.25	V
Input offset voltage	9–10				10	mV

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
PROTECTION AND STABILIZATION CIRCUIT						
(For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
Negative bias present	12				–4.2	V
No Negative protection disabled	12		2.5			V
Regulation level	12		–5.4	–5.0	–4.6	V
Sink current	12				5.0	MA
STEERING SWITCHES, SERIES RESISTANCE						
(For typical values T_A = 25°C, for min/max values T_A = –40°C to +85°C, Max T_J = 125°C unless otherwise noted)						
GSM–900 @ Id = 1mA, Vbat = 5.5V	3			60	160	Ω
DCS–1800 @ Id = 1mA, Vbat = 5.5V	4			60	160	Ω
Power Amplifier Startup @ Id = 50mA, Vbat = 5.5V	5			1.0	2.0	Ω

Lack of negative circuitry behavior:

The MC33170 hosts a circuitry that prevents the power modulation startup if the negative bias is not established. However, to accommodate with PAs that do make use of a negative bias, it is possible to connect pin 13 to pin 7 and thus invalidate the protection circuitry. The below sketch details the available levels to fulfil this function



MC33170 operating truth table, pin levels:

TxEN	Band Selection	Common Enable	GSM–900	DCS–1800	PA startup
X	X	0	High–impedance	High–impedance	High–impedance
0	X	1	High–impedance	High–impedance	High–impedance
1	0	1	V_{LDO}–Io.$RDS_{(ON)}$	High–impedance	V_{BAT}–Io.$RDS_{(ON)}$
1	1	1	High–impedance	V_{LDO}–Io.$RDS_{(ON)}$	V_{BAT}–Io.$RDS_{(ON)}$

Io is the current delivered by the considered pin, RDS(ON) is the switch series resistance as defined in the section Steering Switches

TYPICAL OPERATING CHARACTERISTICS

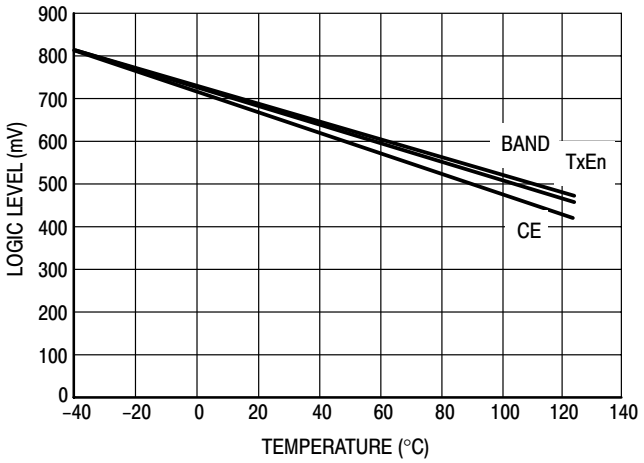


Figure 1. TxEn, BAND, CE Logic Level with Temperature

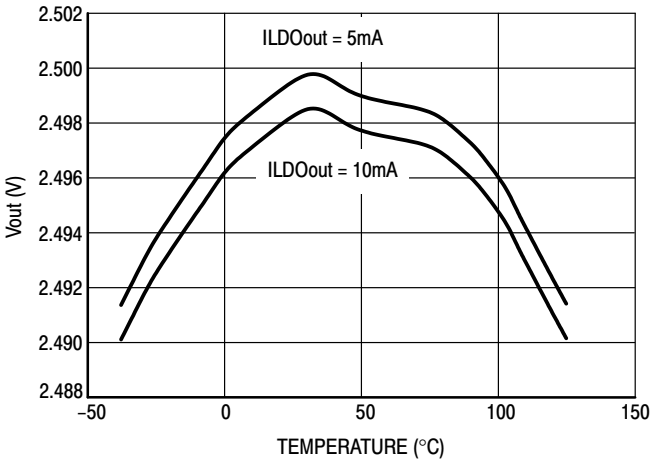


Figure 2. LDO Voltage Output Variation with Temperature

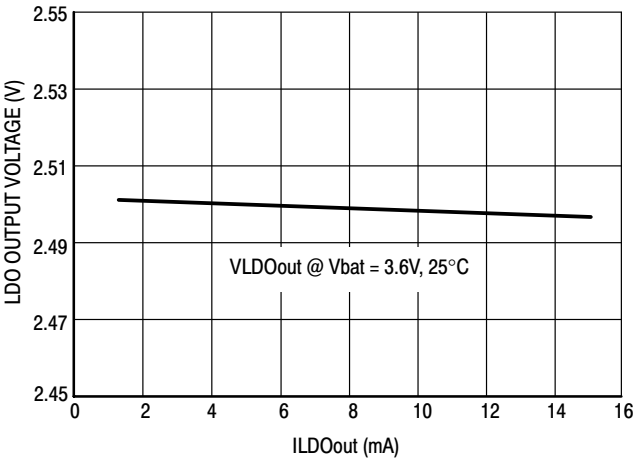


Figure 3. LDO Output Voltage versus LDO Output Current @ 25°C

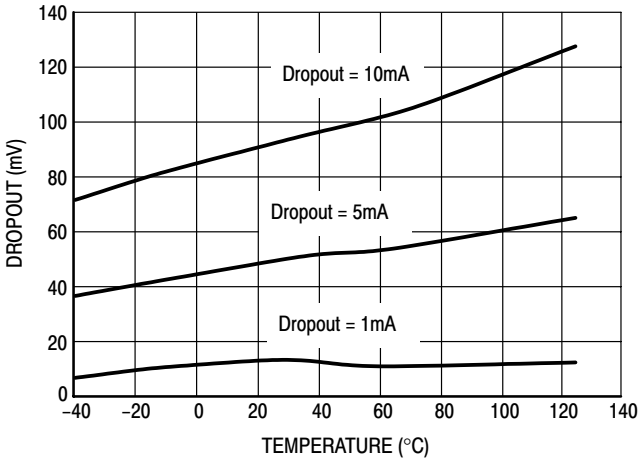


Figure 4. LDO Dropout versus ILDOout Current @ 25°C

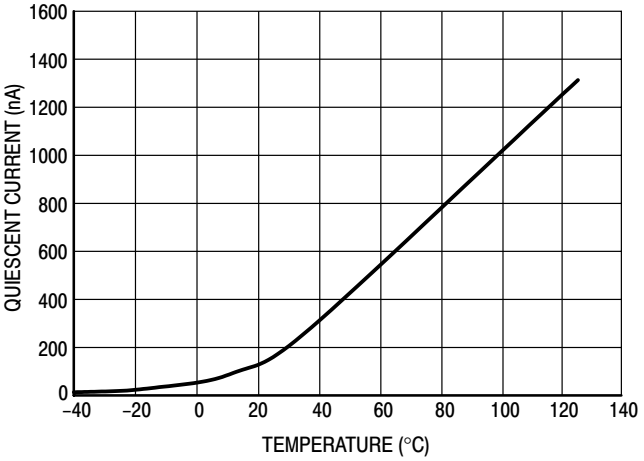


Figure 5. Quiescent Current versus Temperature

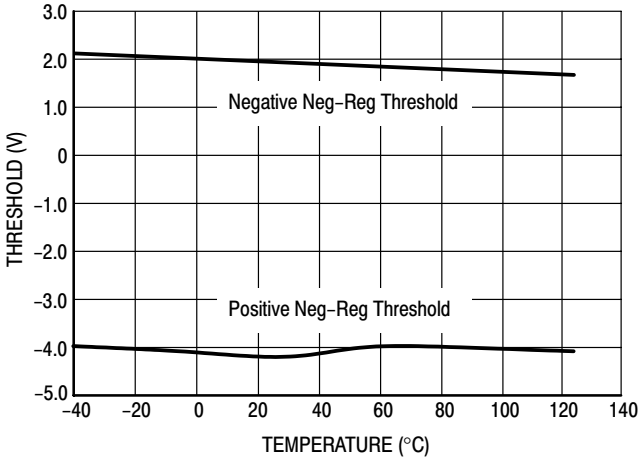


Figure 6. Neg−Reg Thresholds versus Temperature

TYPICAL OPERATING CHARACTERISTICS (cont.)

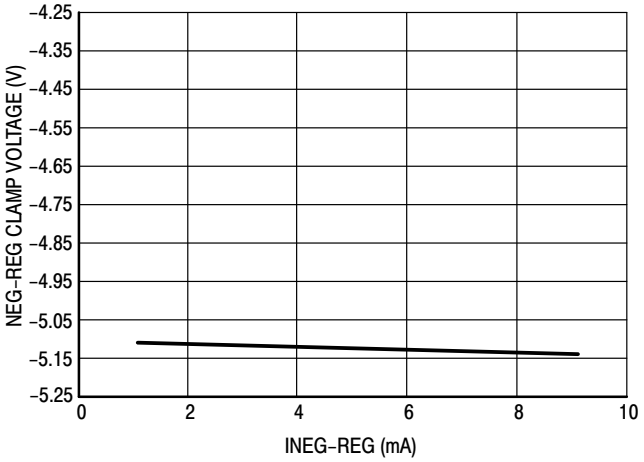


Figure 7. Clamp Voltage vs INeg−Reg Current @ 25°C

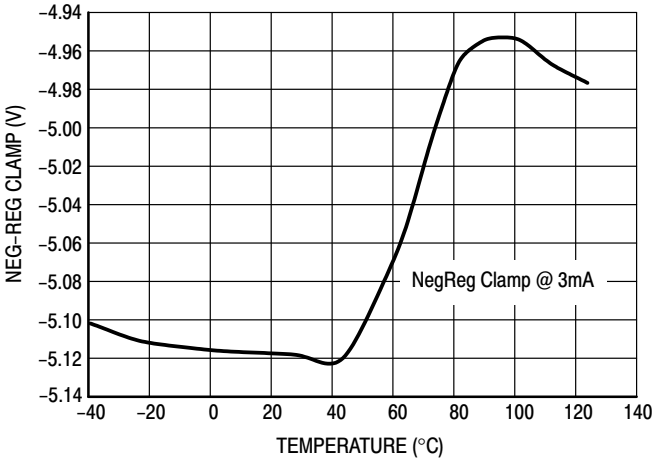


Figure 8. NegReg Clamp @ 3mA versus Temperature

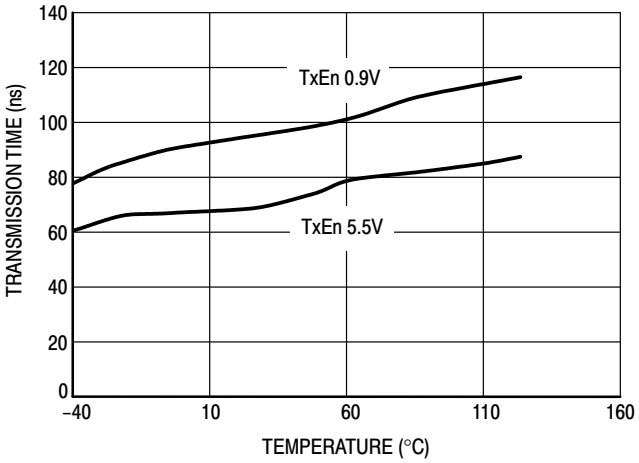


Figure 9. Transmission Enable Propagation Delay versus Temperature

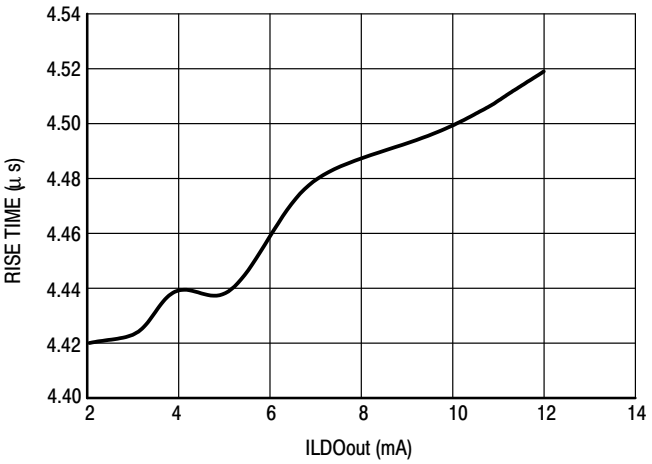


Figure 10. LDO Rise Time versus Load @ 25°C

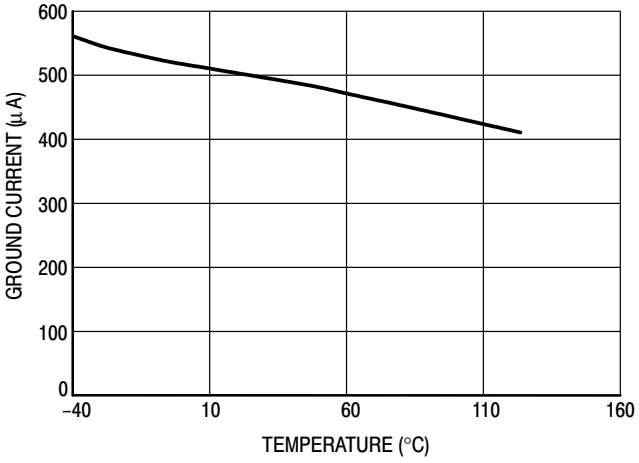


Figure 11. Ground Current versus Temperature

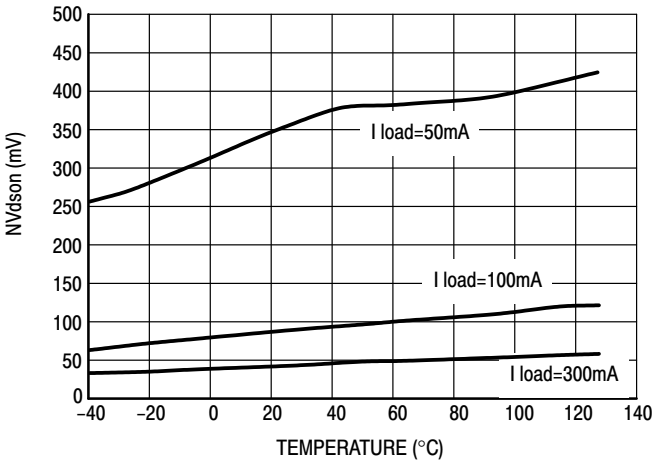
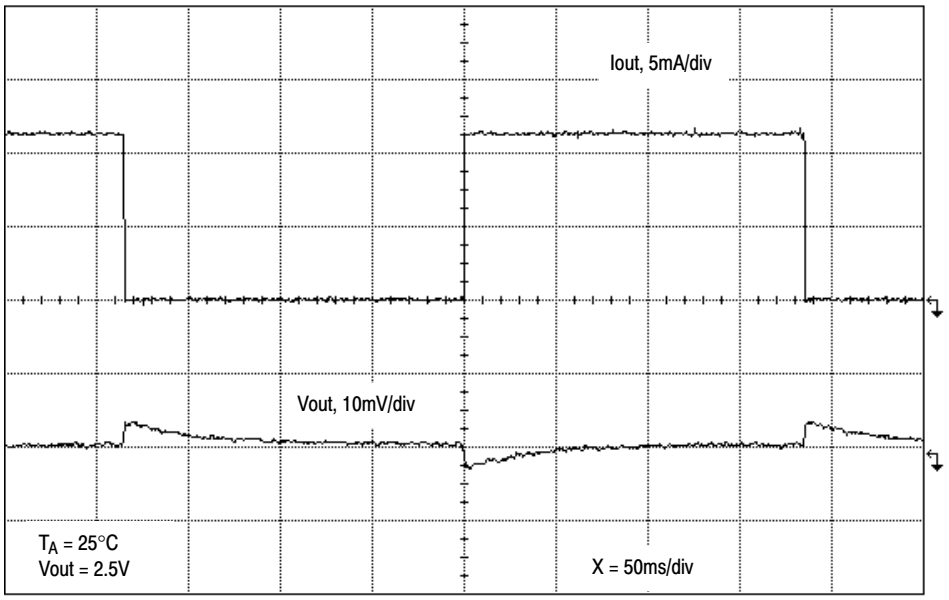
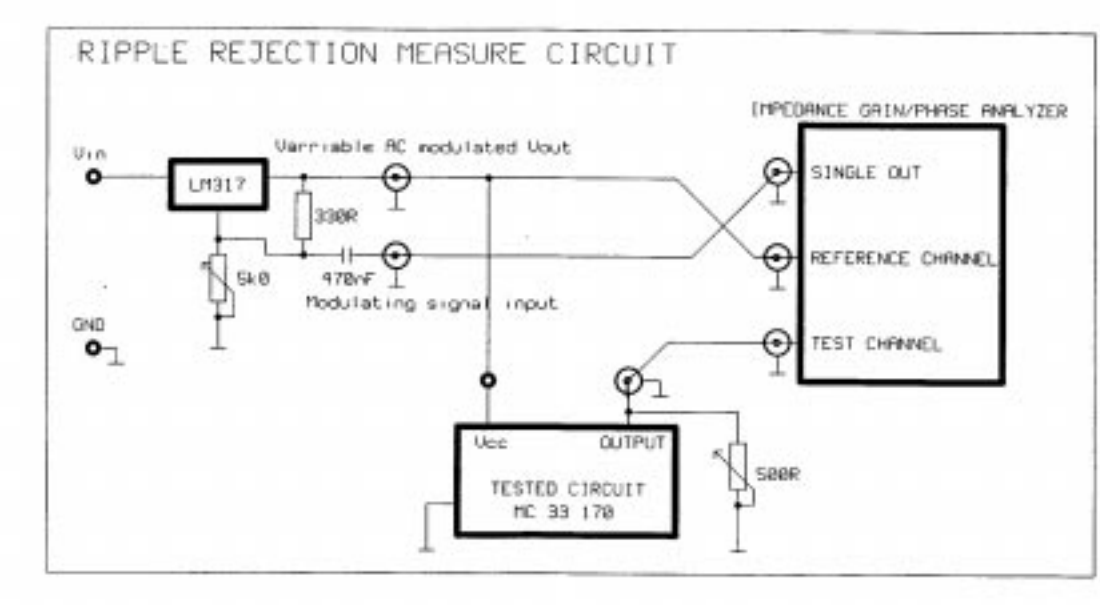


Figure 12. PA Start up Vdson @ Vbat 3.6V

CHARACTERIZATION CURVES

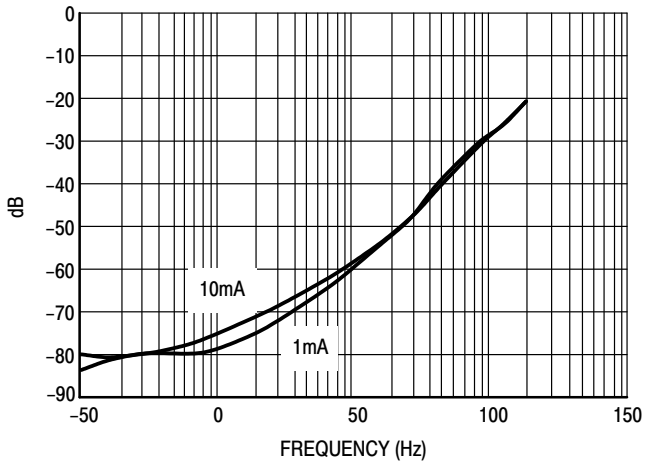


LDO's output when banged from 0 to 10mA



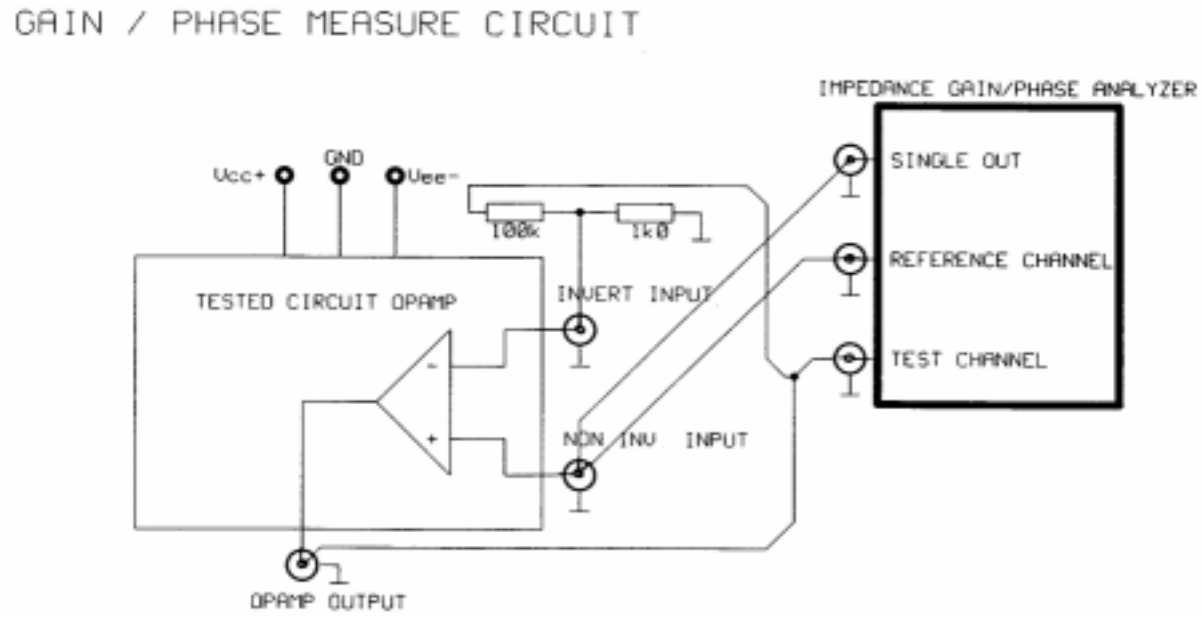
Audio susceptibility measurement fixture

Measurement conditions:
Tx = CE = 1.0V, Vcc = 3.6V, NegOut = Vcc, Cbyp = 100nF

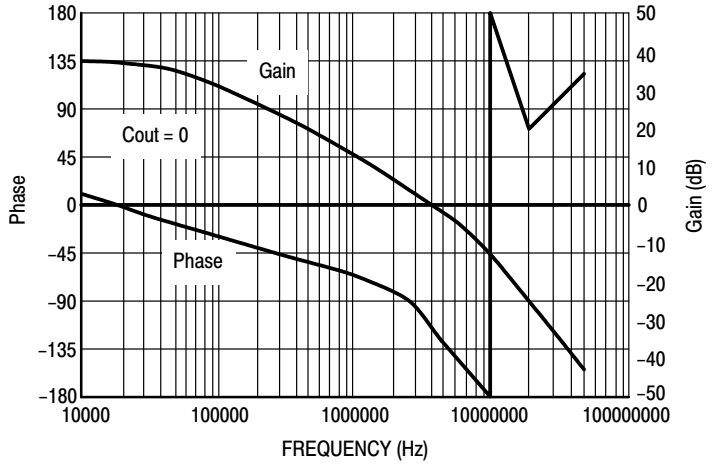


Input voltage rejection at Iout = 1mA and 10mA

Input audio susceptibility at Iout = 1mA/10mA

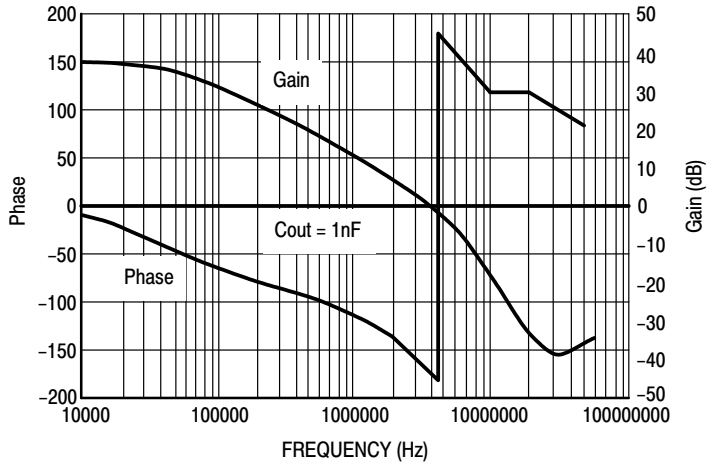


Gain/phase measurement fixture



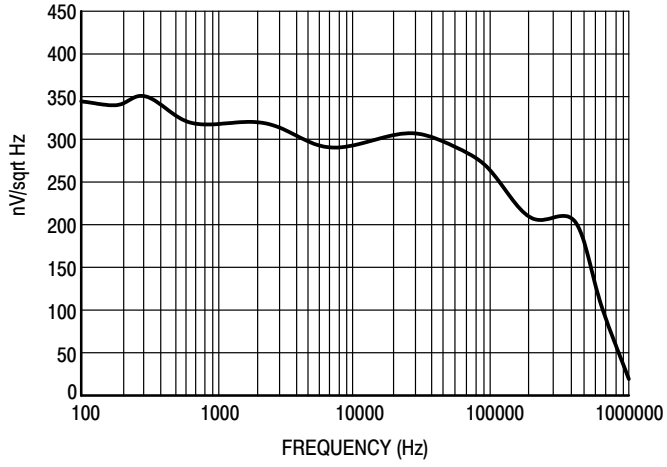
MC33170 Bode plot

Operational amplifier AC measurements with:
Vcc = 3.6V, Tx = CE = 1.0V, Vboost = 8V,
Pin 12 loaded ***not*** loaded



MC33170 Bode plot

Operational amplifier AC measurements with:
Vcc = 3.6V, Tx = CE = 1.0V, Vboost = 8V,
Pin 12 loaded by 1nF



Spectral noise density at Iout = 1mA

LDO output noise measurement with:
Vcc = 3.6V, Tx = CE = 1.0V, Cout = 100nF, Iout = 1mA
Integrated noise: 20Hz – 200kHz = 100μVrms
20Hz – 1MHz = 170μVrms

MC33170 application hints

The MC33170 represents a major leap toward miniaturization and compactness of Power Amplifiers (PAs) systems. Prior to talk about the 33170 application circuits, let us review how a classical dual–band transmission chain is implemented. At the beginning of the chain, the power ramping signal is delivered by the Baseband's Digital to Analog Converter (DAC). Because of the digitization, a natural discontinuity appears between the various steps the signal is made of. As a matter of fact, this sharp transitions create undesirable effects and need to be smoothed by an external circuitry (**figure 13**).

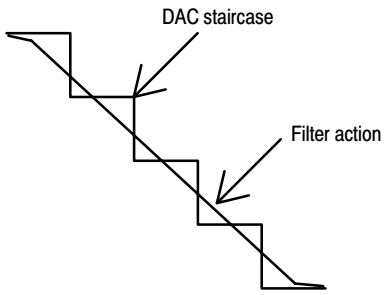


Figure 13. DAC's signal can be smoothed by an appropriate circuitry

The filtering action can be implemented in a various way, but usually a 3rd order Bessel filter represents a good choice. Actual solutions require the use of an external operational amplifier (OPAMP) dedicated to this function.

For drain–controlled PAs, the power is directly dependent upon the supply delivered to the device. Several methods exist but the preferred one stays the N or P channel modulation. In this application, the N–channel is wired in a source–follower configuration and therefore needs an external voltage to ensure its adequate enhancement. This upper voltage can be obtained from a step–up converter or directly from ON Semiconductor PAs, as with the MRFIC0919 or MRFIC1819. To quickly charge/discharge the MOSFET Ciss capacitor, a dedicated driver is needed, with a voltage swing high enough to bias the N–channel toward its specified RDSON.

Radio–Frequency PAs need stable bias levels to keep their operating point at the right place, despite supply variations. A Low DropOut (LDO) regulator is the obvious choice for this purpose. Unfortunately, to keep the quiescent power at its minimum during the GSM/DCS time–frame pauses (e.g. no power delivered), it is important to quickly remove the bias from the PAs. Conversely, the LDO shall be fast enough to bias the PAs at anytime, without hampering the overall response time. Such a task is difficult for an off–the–shelf regulator: a specific component has to be found.

Thanks to their innovative designs, ON Semiconductor PAs, such as the aforementioned ones, do not require any external negative sources. However, some synchronization signals are needed to activate the internal circuitry and provide them with a stable operating point. This is usually done by using external low/high power switches.

Finally, a safety system needs to be implemented to prevent the modulation start in case the negative bias is not established.

Gathering all these information onto a final drawing gives birth to **figure 14**.

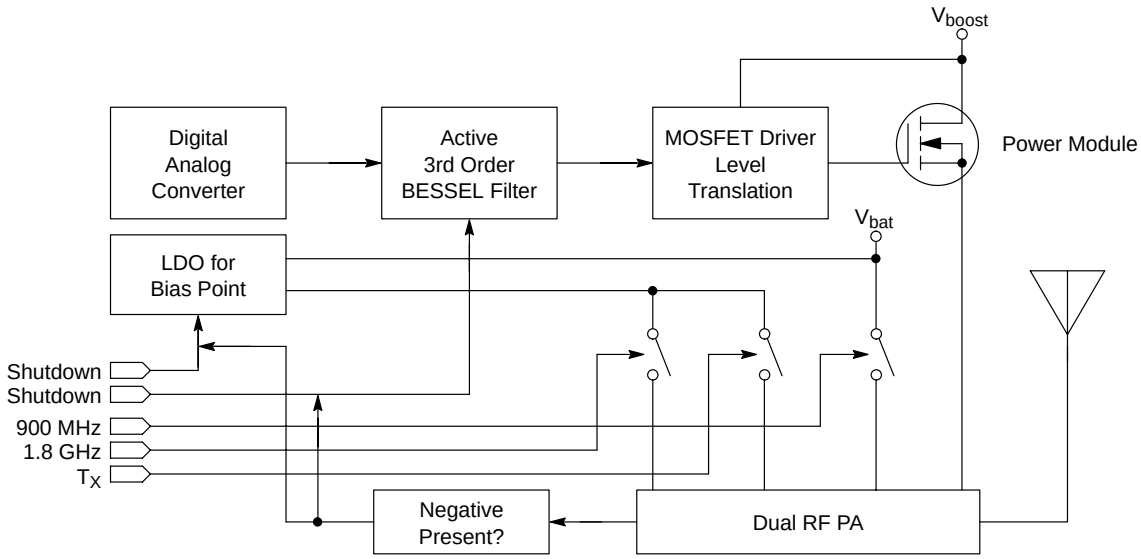


Figure 14. Actual solution to drive a two–PA configuration

MC33170 as a Bessel filter

Thanks to its package, the MC33170 simplifies the implementation of any filtering/driving configuration, e.g. with either an N or P–channel MOSFET. **Figure 15a** details the way to wire a 100kHz filter while driving an N–channel MOSFET. In this application, a third order filter is achieved by combining a first pole passive RC–filter, followed by a second–order Sallen–Key complex pole–pair section.

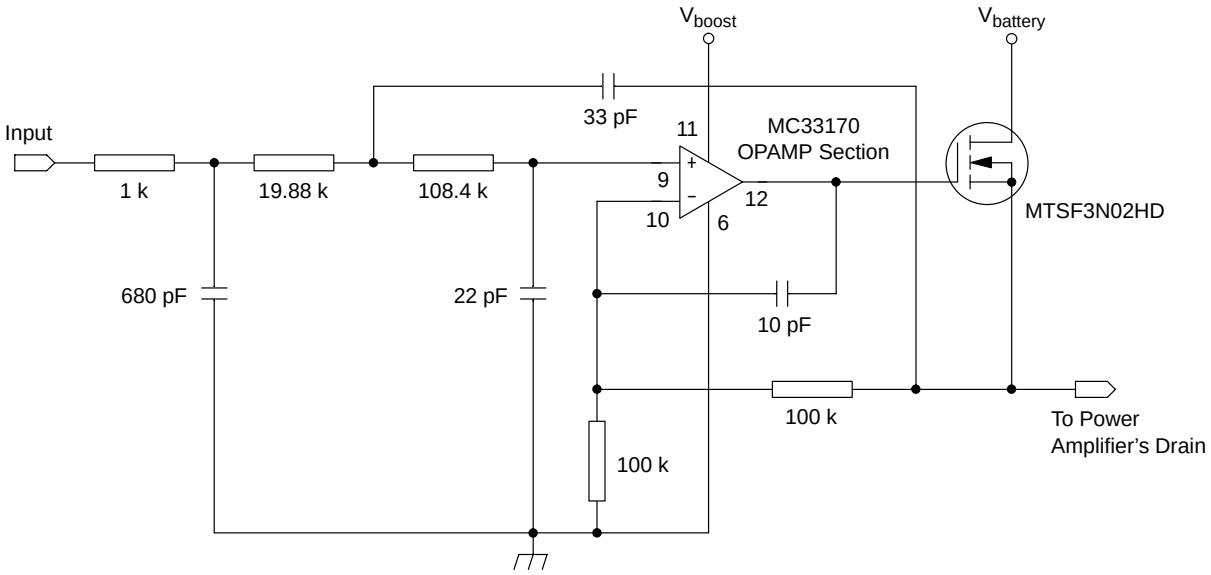


Figure 15a. Using the MC33170's OPAMP to filter out the DAC discontinuities

As one can see, it is easy to select the desired gain value via the 100k feedback resistors and accordingly tailor it to the DAC output level. Figure 15a performs the filtering function but also delivers the adequate sink/source current to drive the MOSFET transistor. The two–component section of figure 2 is reduced into a single one, saving cost and PCB area. It also important to point out that the OPAMP section can be totally disabled by the Common Enable pin.

Benefits of the closed loop configuration

One of the MC33170's key applications is to make the modulation section operating in a closed–loop configuration. That is to say, the power chain is closed through the feedback resistor (the 100kΩ network in figure 3) and forces the output to follow the input ramp. With N–channels, it brings several benefits:

1. The input ramp does no longer deals with the MOSFET threshold voltage which can introduce a certain amount of delay in the response time.
2. At low powers, the distributions between the $RDS_{(ON)}$ is automatically compensated.

With P–channels, the application does not need an elevated voltage to ensure the channel enhancement but maximizes the presence of the OPAMP to ensure a fully linear chain.

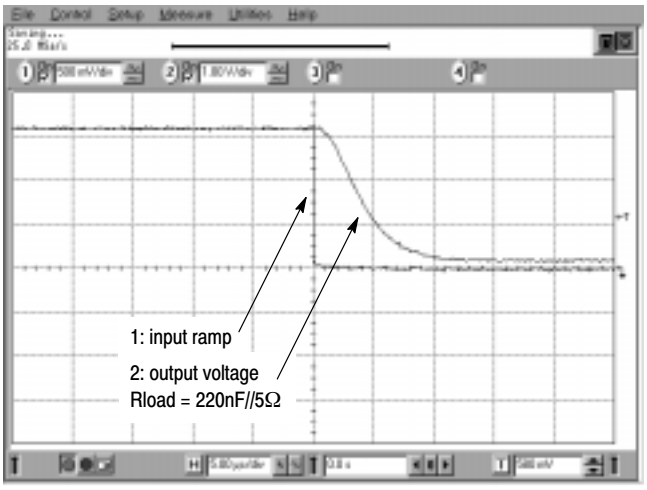


Figure 15b. Going down with the 100kHz filter

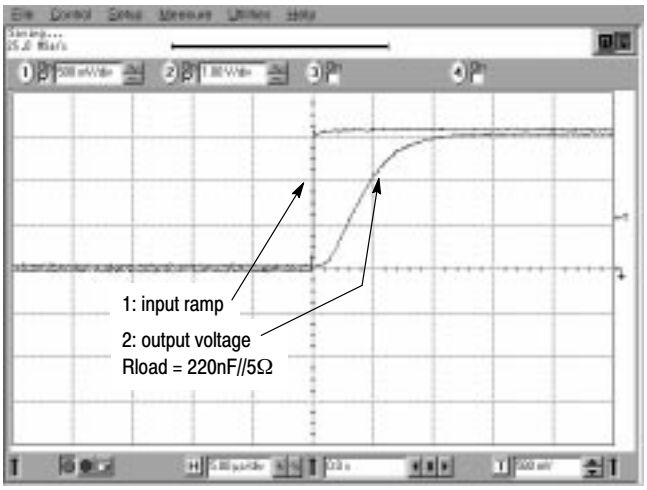


Figure 15c. Going up with the 100kHz filter

The need of a fast regulator

Since the internal LDO controls the PA's bias points, it is important to quickly drive the regulator in order to ensure the minimum consumption during the non–modulation phases. A standard LDO has difficulties to react in less than 30µs. This delay would be unacceptable in a system operating with fast frames. The MC33170 internal LDO has be designed to react within less than 10µs, ensuring a prompt bias establishment. Figure 16 shows the way the bias voltage takes place, without any overshoot.

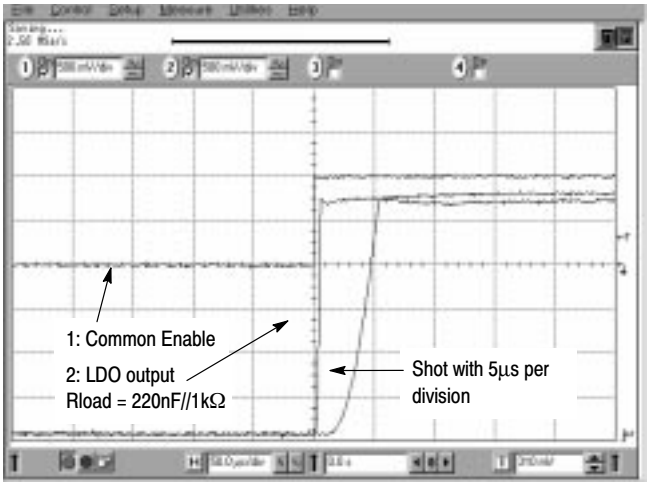


Figure 16. A fast LDO ensures an immediate bias availability

The LDO requires a standard 100nF decoupling capacitor to keep its output stable. The typical output noise stays within 100µV from 100Hz to 100kHz.

High and low current switches

The MC33170 hosts two types of steering switch. The first one only deals with low currents since it delivers the operating bias voltage to the PAs. With two distinct switches, the MC33170 low–current switches control the RF PA GSM 900MHz or DCS 1.8GHz. Once again, the reaction time of these elements is optimized to ensure a fast operation. Figure 17a depicts the typical signal variations. Please note that the Tx pin is controlled via a logic 0 1 of 1V ensuring the compatibility with 1V platforms.

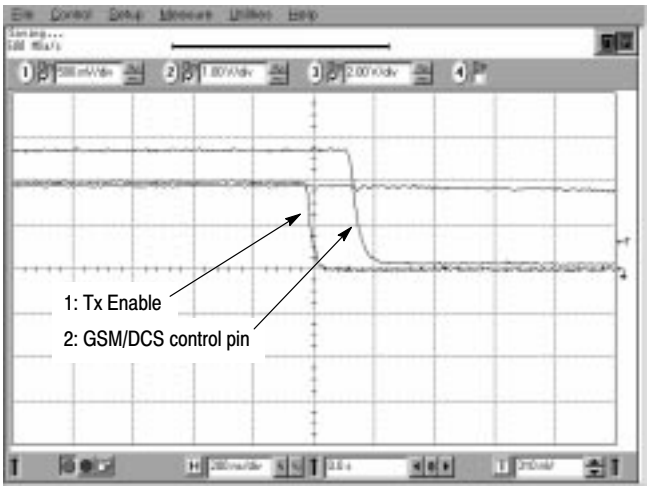


Figure 17a. Typical GSM/DCS pins response time

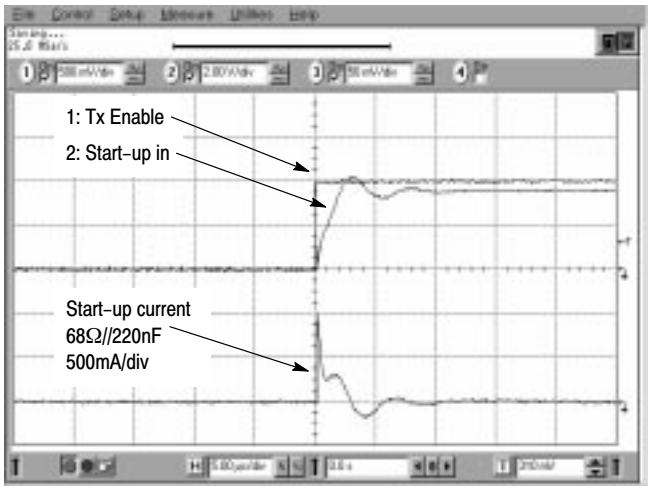


Figure 17b. Peak current capability of the power switch

Complete dual–band application

Figure 18 shows how implementing the MC33170 in a complete dual–band application where a 100kHz filter is combined with the MOSFET driver.

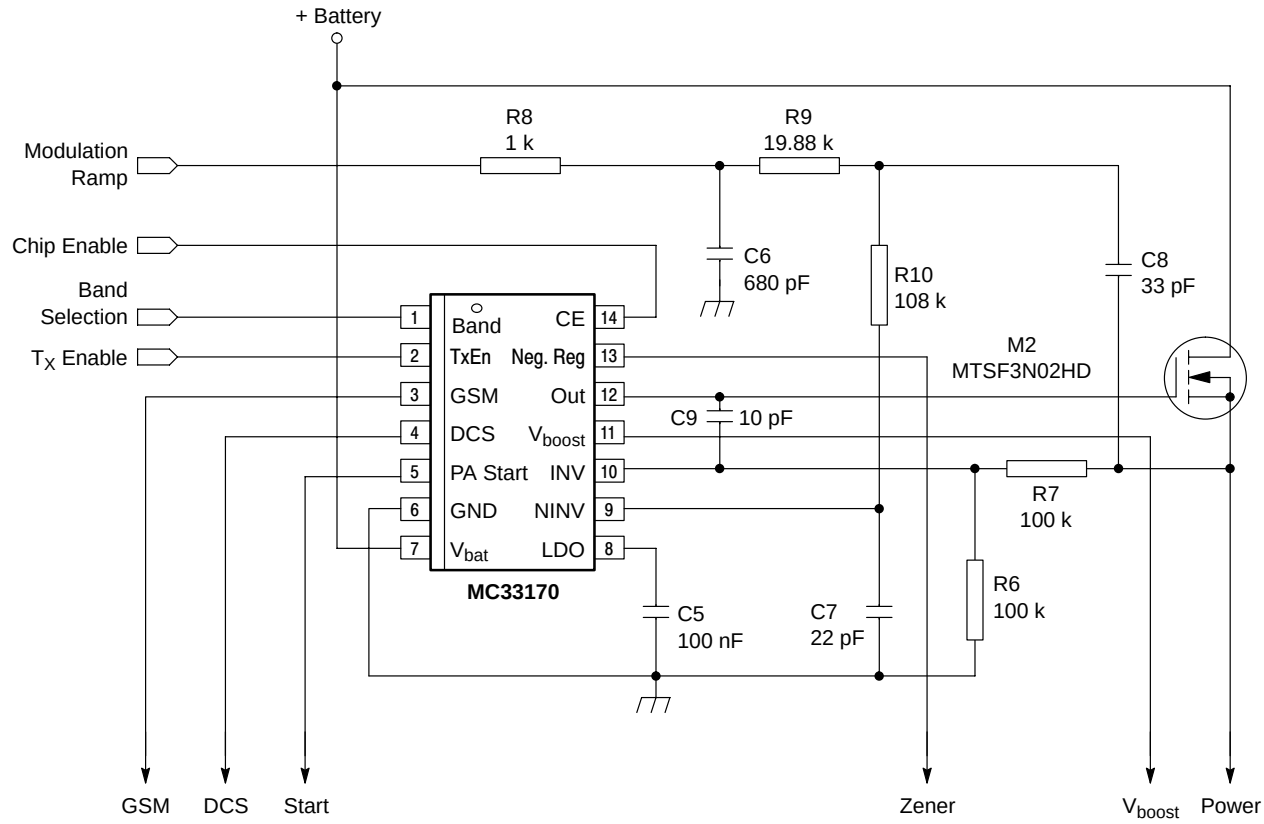


Figure 18. A complete dual–band application with the MC33170

Application

The MC33170 has been designed to fulfill the requirements of the new ON Semiconductor dual–band RF amplifier, the MRFIC1859. For demonstration purposes, the device was driven by the MC33170 in a simple gain two configuration. The below picture shows how the power signal drives the PA's drain.

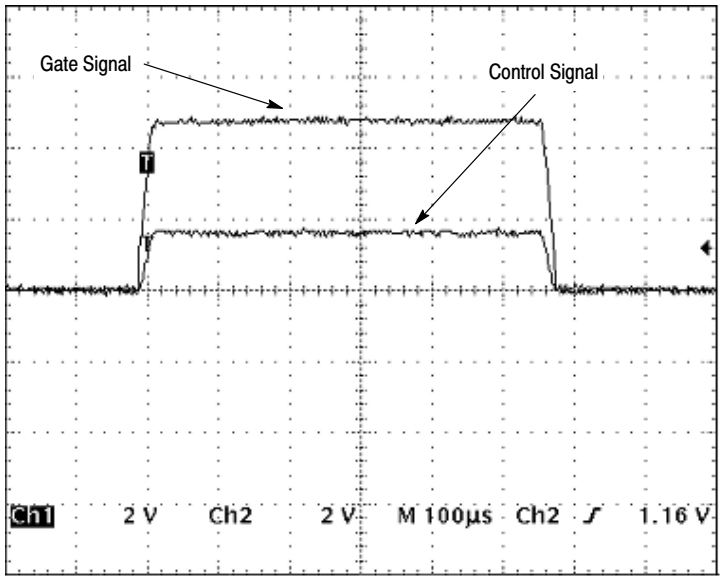


Figure 19. The driving signal delivered by the MC33170 allows fully linear power modulation

GSM specifications

In order to meet the GSM specifications, the modulation edges must be smoothed to fit into the spectral template. This can be accomplished by implementing figure 18's Bessel filter and adjusting the cutoff frequency. Once the edges are smoothed, the complete systems nicely fits into the GSM template, as depicted by **figure 20**.

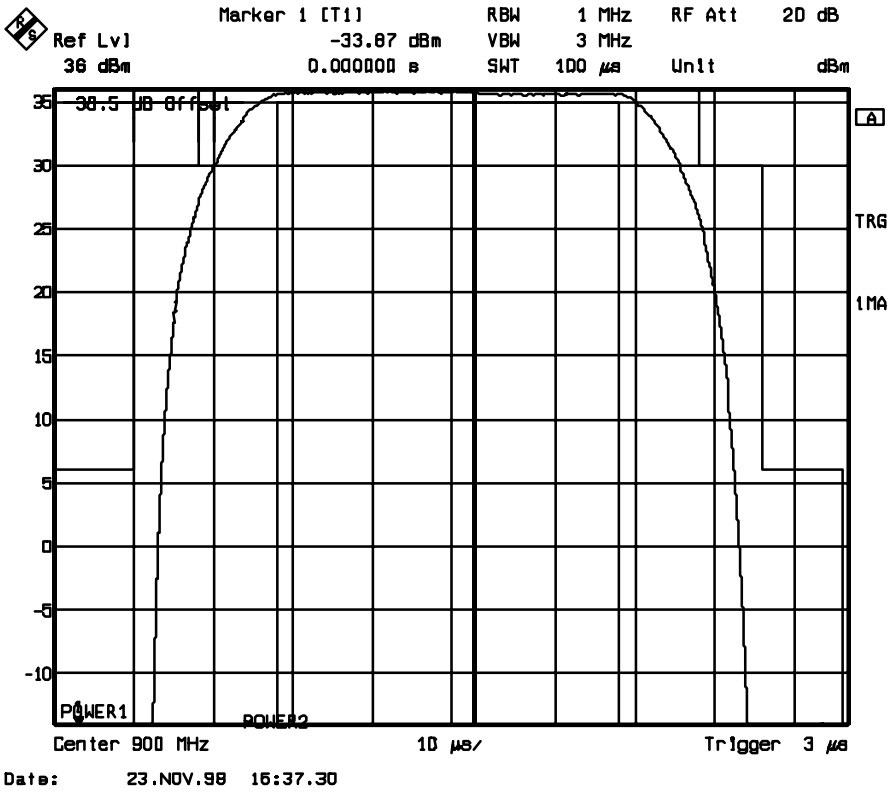
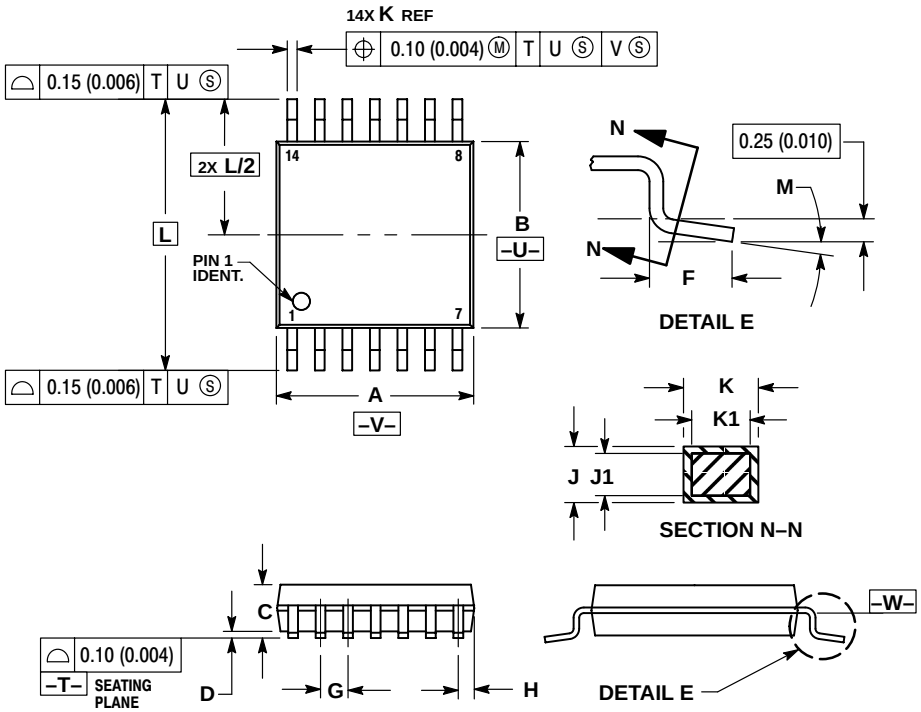


Figure 20. Thanks to its flexibility, the MC33170 helps reaching the GSM specs

PACKAGE DIMENSIONS

TSSOP–14
DTB SUFFIX
PLASTIC PACKAGE
CASE 948G–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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