PACIFIC MONOLITHICS®

A Division of Richardson Electronics

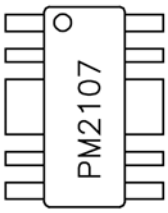
PM 2107

DATA SHEET

RFIC Power Amplifier
2400 to 2500 MHz Operation

Features

- **30 dBm Output Power**
- **45% Efficiency**
- ***NEW* 10 Pin PM-SOP™ Package**
- **Low Profile, PCMCIA Type II Compatible**
- **Small Size (Half the Footprint of SO-14)**
- **No Bottom Side Contact**



PM-SOP™
Plastic Package

Applications

- **2400 MHz ISM Band Transmitters**
- **2 GHz Wireless Local Loop Systems**

Description

The PM2107 is a small outline plastic packaged high efficiency GaAs RFIC power amplifier developed for applications in the 2400 MHz ISM band. This two stage RFIC amplifier is off-chip matched to provide optimum performance for a variety of applications. Operating from a 5 volt supply, the PM2107 can produce 1 watt of saturated output power with 45% typical efficiency. Matching networks and performance characteristics are provided in this data sheet for 2.4 to 2.5 GHz operation. Schematics and layouts for other applications are available upon request from Pacific Monolithics.

Electrical Characteristics

V_{DD}= 5.0V, V_{GG1} = -1.2 V, V_{GG2} = -2.1V, T_A = +25°C

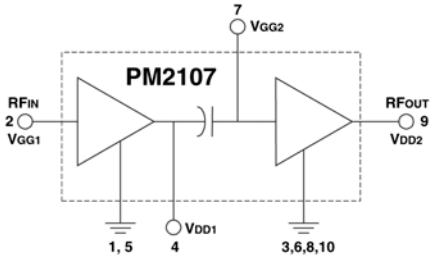
Tested in 50 Ω system, using external circuit shown on page 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency Range	f		2400		2500	MHz
Power Output	P_{SAT}	P_{IN} = 8 dBm	29	30		dBm
Power Added Efficiency	η	P_{IN} = 8 dBm	40	45		%
Small Signal Gain	G			26		dB
Input Return Loss	S_{11}			15		dB
Output Power at 1dB Comp.	P_{1dB}			29		dBm
Operating Drain Current	I_{DD}	$P_{OUT} = P_{SAT}$		440		mA
Gate Current	I_{GG}	$P_{OUT} = P_{SAT}$		0.5	2	mA
Load VSWR for Output Stability[1]	VSWR	Source VSWR < 1.2:1		6:1		
Thermal Resistance	θ_{JC}	Junction to GND lead		40		°C/W

[1] Unconditionally stable (input and output), except for 1.8 GHz < f < 2.4 GHz.

Absolute Maximum Ratings

Characteristics	Symbol	Value	Units
Drain Voltage	$V_{DD1,2}$	+9.0	V
Gate Voltage	$V_{GG1,2}$	-5.0	V
Bias Current	I_{DS}	900	mA
RF Input Power	P_{IN}	+20.0	dBm
Power Dissipation	P_{DISS}	1.6	W
Operating Temperature	T_{OP}	-40 to +85	°C
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

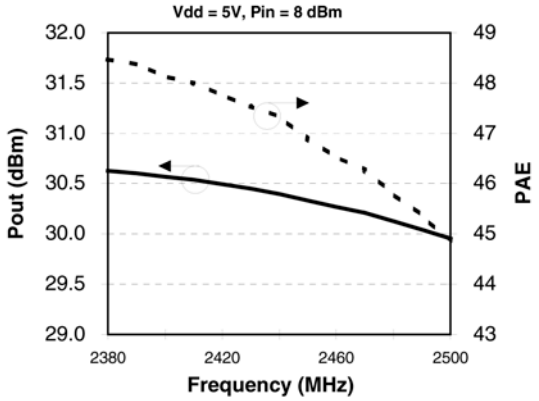


Caution: Operating beyond the specified rating for any of these parameters may cause permanent damage to device.

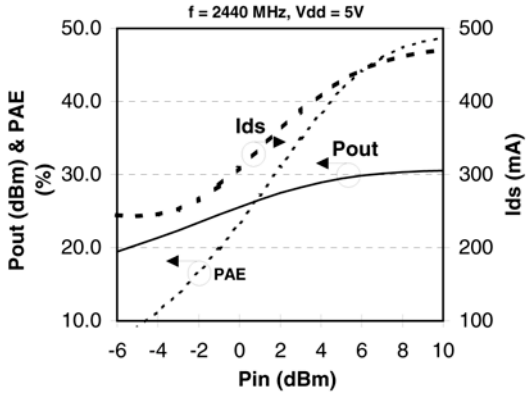
Typical Performance Characteristics

(Obtained using external circuit shown on page 3)

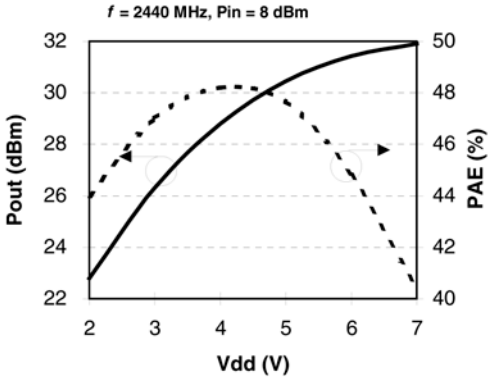
Output Power and Efficiency vs. Frequency



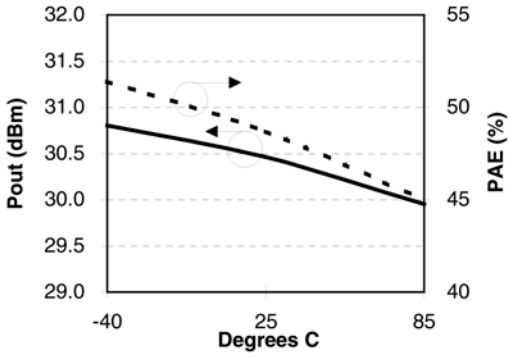
Output Power, Efficiency, and Current vs. Input Power



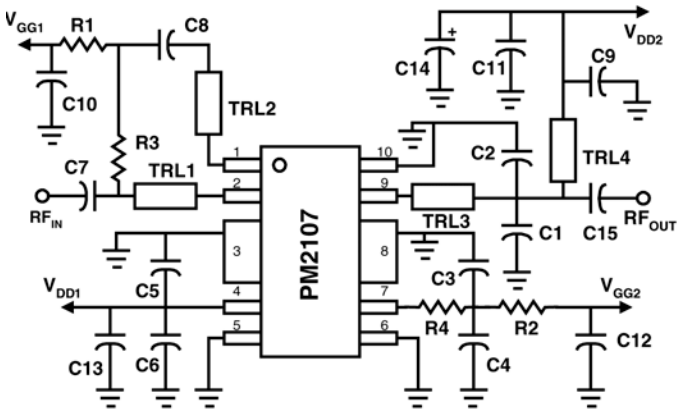
Output Power and Efficiency vs. Supply Voltage



Output Power and Efficiency vs. Temperature



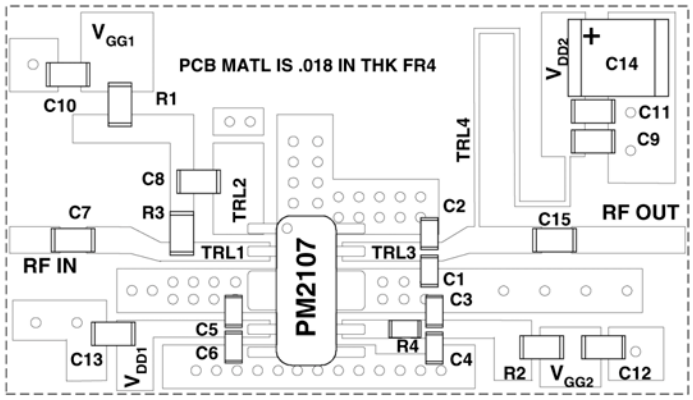
Application Information



Matching Circuit for 2.4 to 2.5 GHz Saturated Operation.

Part	Value / Type	Size
C1	1.2 pF NPO	0402
C2	1.5 pF NPO	0402
C3, C4, C5, C6	33 pF NPO	0402
C7, C8, C9, C15	33 pF NPO	0603
C10, C11, C12, C13	1000 pF X7R	0603
C14	6.8 µF TANT	1206
R1	51 Ω	0603
R2	43 Ω	0603
R3	8.2 Ω	0603
R4	9.1 Ω	0402
TRL1, TRL3	$\theta = 9°$, $Z_0 = 65\ \Omega$	@ 2.44 GHz
TRL2	$\theta = 10°$, $Z_0 = 30\ \Omega$	@ 2.44 GHz
TRL4	$\theta = 90°$, $Z_0 = 105\ \Omega$	@ 2.44 GHz

Pins 2, 4, 7, and 9 are all "RF-hot," and require matching networks or bypass circuits as shown in the schematic above. 0402 size capacitors are recommended for high frequency matching to reduce series inductance. A maximum FR4 board thickness of 18 mils is recommended to minimize via and trace inductances. Large value bypass capacitors shown (1000 pF and greater) need not be located close to the PM2107, but must be present in the circuit to insure low frequency stability. R3 and R4 improve inband stability, and R1 and R2 provide out-of-band stability. The area beneath the amplifier and the associated matching networks must have a continuous ground plane. The fused lead pins 3 and 8 provide a low inductance source ground for the 2nd stage of the PM2107. The inductance to the microstrip ground plane should be as low as possible in grounding these pins. Pin 1 should be grounded through a transmission line to achieve the required input match and improve inband stability. The other ground pins (5, 6, 10) should also be connected to ground through a low inductance path. A lossy input match is formed by TRL1, TRL2, C8, and R3. TRL2 provides ground isolation between the two stages to improve stability. The output matching network consists of TRL3, C1, and C2. Paralleling capacitors is recommended to reduce series inductance. Interstage matching networks consist of bypass capacitors C3-C6 that provide RF grounds for pins 4 and 7.



PCB Layout Information

A recommended layout is shown here. This layout was developed for multiple frequencies of operation, and not space optimized for 2.4 GHz applications. The placement of C1-C6, R3, and R4 are critical with respect to the IC package and the TRL's. Care should be taken to preserve trace lengths as shown in the layout. All other components and traces may be moved to accommodate layout constraints.

Approximate Scale: 5:1

Biasing

The negative gate bias supplies should always be applied before the application of the positive drain supply voltage. Damage is likely to occur if negative supplies are not turned on within 20 msec after the positive supply turn-on. Care must be taken to insure that time constants on the gate supply lines are not substantially longer than those on the drain supplies. The second stage gate (pin 2) can draw up to 2 mA of forward (into the gate) current at full output power. Charge pump circuits must be able to source this much current, and isolation resistors must be kept below 100Ω to avoid a shift in negative bias voltage. Although the PM2107 can withstand a 14 V gate-drain reverse potential, we recommend a maximum operating supply voltage of 6V for efficient operation.

Thermal Considerations

The fused leads (pins 3, 8) on the PM2107 provide most of the thermal path from the device junction. In the absence of other heat conducting structures, we recommend 3 sq-in of continuous copper ground plane per watt of dissipated power (Note: P_{DISS} = Duty Cycle × (P_{DC} - P_{RF})). 2 oz. copper is recommended for the ground plane layer, with a minimum of 20 via holes to the component side in close proximity to the ground leads.

Package Specifications

Pin Connections

Pin Number	Function
1	GND
2	RF_{IN}/V_{GG1}
3	GND
4	V_{DD1}
5	GND
6	GND
7	V_{GG2}
8	GND
9	RF_{OUT}/V_{DD2}
10	GND

PM-SOP™ Outline Drawing