DATA SHEET

CGY2014ATW
GSM/DCS/PCS power amplifier

Preliminary specification
File under Integrated Circuits, IC17

2000 Nov 28

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GSM/DCS/PCS power amplifier CGY2014ATW

FEATURES

- Operates at 3.6 V battery supply voltage
- Power Amplifier (PA) output power: 35 dBm in GSM band and 32.5 dBm in DCS/PCS band
- Input power: 5 dBm in GSM band and DCS/PCS band
- Wide operating temperature range from T_{amb} = –20 to +85 °C
- HTSSOP20 exposed die pad package.

APPLICATIONS

- Dual-band systems: Low Band (LB) from 880 to 915 MHz hand-held transceivers for E-GSM and High Band (HB) from 1710 to 1910 MHz for DCS/PCS applications.

GENERAL DESCRIPTION

The CGY2014ATW is a dual-band GSM/DCS/PCS GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier. The circuit is specifically designed to operate at 3.6 V battery supply voltage.

The power amplifier requires only a 30 dB harmonic low-pass filter to comply with the transmit spurious specification.

The voltages applied on pins V_{DD} (drain) control the power of the power amplifier and enable it to be switched off.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	–	3.5	5.2	V
$I_{DD(LB)}$	GSM positive peak supply current	–	2	–	A
$P_{o(LB)(max)}$	maximum output power in GSM band	34.5	35	–	dBm
$I_{DD(HB)}$	DCS/PCS positive peak supply current	–	1.5	–	A
$P_{o(HB)(max)}$	maximum output power in DCS/PCS band	32	32.5	–	dBm
T_{amb}	ambient temperature	–20	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2014ATW	HTSSOP20	plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm	SOT527-1

BLOCK DIAGRAM

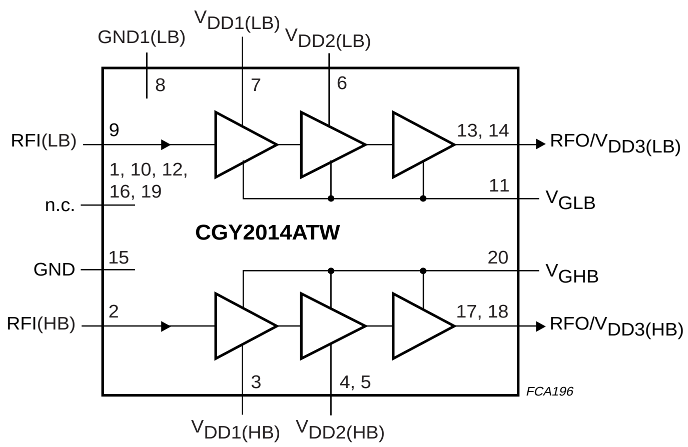


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
RFI(HB)	2	DCS/PCS power amplifier input
$V_{DD1(HB)}$	3	DCS/PCS first stage supply voltage
$V_{DD2(HB)}$	4	DCS/PCS second stage supply voltage
$V_{DD2(HB)}$	5	DCS/PCS second stage supply voltage
$V_{DD2(LB)}$	6	GSM second stage supply voltage
$V_{DD1(LB)}$	7	GSM first stage supply voltage
GND1(LB)	8	GSM first stage ground
RFI(LB)	9	GSM power amplifier input
n.c.	10	not connected
V_{GLB}	11	GSM power amplifier gates
n.c.	12	not connected
RFO/$V_{DD3(LB)}$	13	GSM power amplifier output and third stage supply voltage
RFO/$V_{DD3(LB)}$	14	GSM power amplifier output and third stage supply voltage
GND	15	ground
n.c.	16	internal connection to ground; pin should not be connected to the board
RFO/$V_{DD3(HB)}$	17	DCS/PCS power amplifier output and third stage supply voltage
RFO/$V_{DD3(HB)}$	18	DCS/PCS power amplifier output and third stage supply voltage
n.c.	19	not connected
V_{GHB}	20	DCS/PCS power amplifier gates
–	exposed die	ground

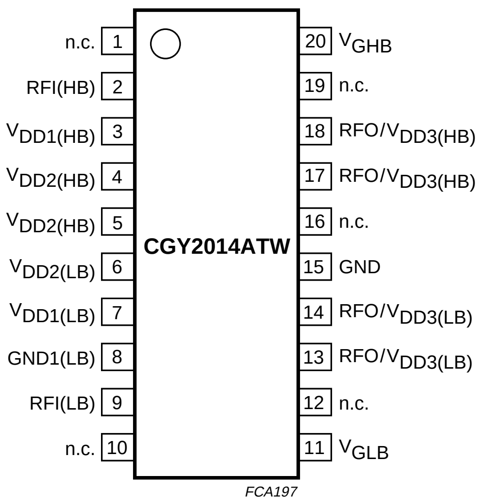


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2014ATW is designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *“ETS 300 577 specification”*, which are defined as follows:

- t_{on} = 570 μs
- T = 4.16 ms
- Duty cycle δ = $^1/_8$.

Multislot operation can be implemented provided that the application circuit does not drive the IC beyond the limiting values.

Power amplifier

The GSM and DCS/PCS power amplifiers consist of three cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DD}	supply voltage		5.2	V
$T_{j(max)}$	maximum operating junction temperature		150	°C
T_{stg}	storage temperature		150	°C
P_{tot}	total power dissipation	note 1	2.0	W
$P_{i(LB)}$	GSM input power		10	dBm
$P_{i(HB)}$	DCS/PCS input power		10	dBm

Note

1. The total power dissipation is measured under GSM pulse conditions in a good thermal environment; see *Application Note* (tbf).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	note 1	30	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions in a good thermal environment; see *Application Note* (tbf).

DC CHARACTERISTICS

V_{DD} = 3.5 V; T_{amb} = 25 °C; measured on the Philips application diagram (see Fig.3); general operating conditions applied; peak current values measured during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: pins $V_{DD1(LB)}$, $V_{DD2(LB)}$, RFO/$V_{DD3(LB)}$, $V_{DD1(HB)}$, $V_{DD2(HB)}$ and RFO/$V_{DD3(HB)}$						
V_{DD}	supply voltage	note 1	0	3.5	5.2	V
$I_{DD(LB)}$	GSM positive peak supply current	$P_{i(LB)}$ = 5 dBm	–	2	–	A
$I_{DD(HB)}$	DCS/PCS positive peak supply current	$P_{i(HB)}$ = 5 dBm	–	1.5	–	A
$I_{DD(lp)(LB)}$	GSM positive supply current	note 2	–	200	300	mA
$I_{DD(lp)(HB)}$	DCS/PCS positive supply current	note 3	–	200	300	mA

Notes

1. The supply circuit includes a (drain) MOS switch with R_{DSon} = 40 mΩ. The battery voltage is 3.6 V (typical).
2. $V_{DD1(LB)}$ = 2.8 V; $V_{DD1(LB)}$ adjusted for $P_{o(LB)}$ = 15 dBm, this adjustment is typically 0.5V.
3. $V_{DD1(HB)}$ = 2.8 V; $V_{DD1(HB)}$ adjusted for $P_{o(HB)}$ = 15 dBm, this adjustment is typically 0.6V.

AC CHARACTERISTICS

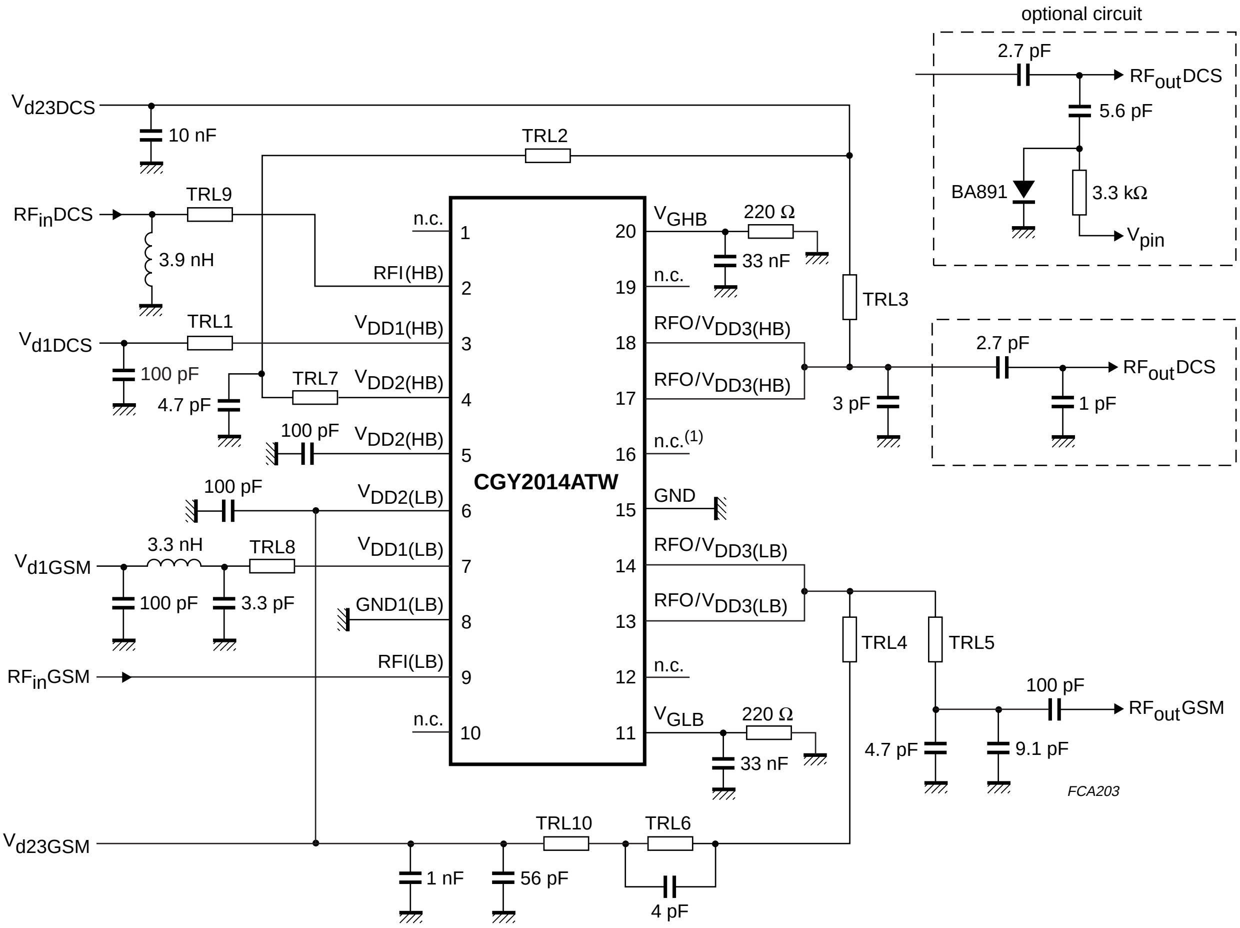
V_{DD1} = 2.8 V; V_{DD2} = V_{DD3} = 3.5 V; T_{amb} = 25 °C; measured on the Philips application diagram (see Fig.3).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Low band: GSM power amplifier						
$P_{i(LB)}$	input power		3	5	7	dBm
$f_{RF(LB)}$	RF frequency range		880	–	915	MHz
$P_{o(LB)(max)}$	maximum output power		34.5	35	–	dBm
η_{LB}	efficiency		50	55	–	%
$P_{o(LB)(min)}$	minimum output power	V_{DD} = 0 V; $P_{i(LB)}$ = 5 dBm	–	–30	–	dBm
$N_{RX(LB)}$	output noise in RX band	$P_{i(LB)}$ = 5 dBm f_{RF} = 925 to 935 MHz f_{RF} = 935 to 960 MHz	 – –	 – –	 –117 –129	 dBm/Hz dBm/Hz
$H2_{LB}$	2nd harmonic level	$P_{i(LB)}$ = 5 dBm	–	–	–35	dBc
$H3_{LB}$	3rd harmonic level	$P_{i(LB)}$ = 5 dBm	–	–	–35	dBc
$Stab_{LB}$	stability	$P_{i(LB)}$ = 5 dBm; note 1	–	–	–60	dBc
High band: DCS/PCS power amplifier; note 2						
$P_{i(HB)}$	input power		3	5	7	dBm
$f_{RF(HB)}$	RF frequency range	for DCS operation	1710	–	1785	MHz
$P_{o(HB)(max)}$	maximum output power		32	32.5	–	dBm
η_{HB}	efficiency		38	40	–	%
$P_{o(HB)(min)}$	minimum output power	V_{DD} = 0 V; $P_{i(HB)}$ = 5 dBm	–	–30	–	dBm
α_{HB}	high band isolation when low band is operating	$V_{DD(LB)}$ = 3.5 V; $P_{i(LB)}$ = 5 dBm; $V_{DD(HB)}$ = 0 V; $P_{i(HB)}$ = 5 dBm; note 3	–	0	–	dBm
$N_{RX(HB)}$	output noise in RX band	$P_{i(HB)}$ = 5 dBm	–	–	–121	dBm/Hz
$H2_{HB}$	2nd harmonic level	$P_{i(HB)}$ = 5 dBm	–	–	–35	dBc
$H3_{HB}$	3rd harmonic level	$P_{i(HB)}$ = 5 dBm	–	–	–35	dBc
$Stab_{HB}$	stability	$P_{i(HB)}$ = 5 dBm; note 1	–	–	–60	dBc

Notes

1. The device is adjusted to provide nominal load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.
2. The power amplifier can be matched to PCS and/or DCS/PCS operation through optimization of the matching circuit; see *Application Note* (tbf).
3. Isolation can be improved to –20 dBm (typical) with a pin diode switched in the DCS output matching circuit.

APPLICATION INFORMATION



(1) Pin 16 is internally connected to ground and should not be connected to the board.

(2) Transmission lines:

Thickness 0.4 mm, substrate FR4 and $\varepsilon_r = 4.7$.

TRL1: width = 500 µm, length = 4.5 mm.

TRL2: width = 500 µm, length = 15 mm, thickness = 1.6 mm.

TRL3: width = 300 µm, length = 32 mm.

TRL4: width = 350 µm, length = 4 mm.

TRL5: width = 800 µm, length = 1.5 mm.

TRL6: width = 450 µm, length = 13 mm.

TRL7: width = 500 µm, length = 2.5 mm.

TRL8: width = 300 µm, length = 2.5 mm.

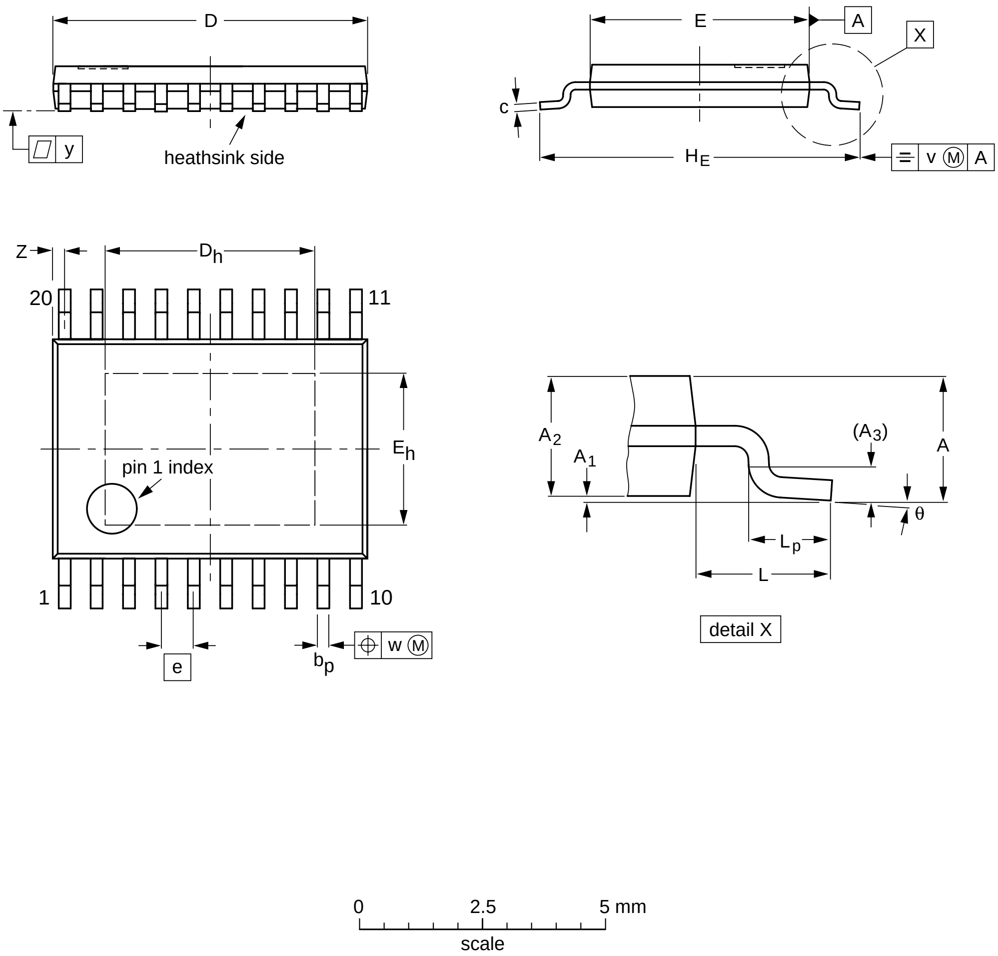
TRL9: width = 800 µm, length = 5 mm.

TRL10: width = 450 µm, length = 2 mm.

Fig.3 Application diagram.

PACKAGE OUTLINE

HTSSOP20: plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm **SOT527-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.20 0.09	6.6 6.4	4.3 4.1	4.5 4.3	3.1 2.9	0.65	6.6 6.2	1.0	0.75 0.50	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT527-1						~~99-11-12~~ 00-07-12

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW[1]**
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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