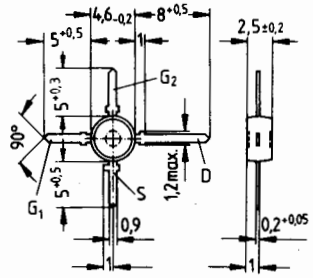
SIEMENS

Silicon N-Channel MOSFET Tetrode — BF 988

- Short-channel transistor with high S/C quality factor
- For low-noise, gain-controlled input stages up to 1 GHz



X-plast
Approx. weight 0.35 g

Dimensions in mm

Type	Ordering code for versions in bulk
BF 988	Q62702-F36

Maximum ratings	Symbol	Ratings	Unit
Drain-source voltage	V_{DS}	12	V
Drain current	I_D	30	mA
Gate 1/Gate 2 source peak current	$\pm I_{G1/2SM}$	10	mA
Total power dissipation $T_A \leq 60$ °C	P_{tot}	200	mW
Storage temperature range	T_{stg}	–55 ... +150	°C
Channel temperature	T_{ch}	150	°C
Thermal resistance			
Channel – ambient	R_{thJA}	≤ 450	K/W

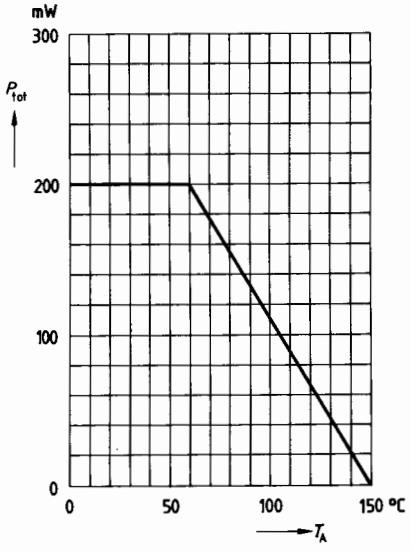
Electrical characteristics
at T_A = 25 °C, unless otherwise specified

DC characteristics	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage I_D = 10 µA, $-V_{G1S} = -V_{G2S}$ = 4 V	$V_{(BR)DS}$	12	–	–	V
Gate 1-source breakdown voltage $\pm I_{G1S}$ = 10 mA, $V_{G2S} = V_{DS}$ = 0	$\pm V_{(BR)G1SS}$	8	–	14	V
Gate 2-source breakdown voltage $\pm I_{G2S}$ = 10 mA, $V_{G1S} = V_{DS}$ = 0	$\pm V_{(BR)G2SS}$	8	–	14	V
Gate 1-source leakage current $\pm V_{G1S}$ = 5 V, $V_{G2S} = V_{DS}$ = 0	$\pm I_{G1SS}$	–	–	50	nA
Gate 2-source leakage current $\pm V_{G2S}$ = 5 V, $V_{G1S} = V_{DS}$ = 0	$\pm I_{G2SS}$	–	–	50	nA
Drain current V_{DS} = 8 V, V_{G1S} = 0, V_{G2S} = 4 V	I_{DSS}	2	–	18	mA
Gate 1-source pinch-off voltage V_{DS} = 8 V, V_{G2S} = 4 V, I_D = 20 µA	$-V_{G1S(p)}$	–	–	2.5	V
Gate 2-source pinch-off voltage V_{DS} = 8 V, V_{G1S} = 0, I_D = 20 µA	$-V_{G2S(p)}$	–	–	2	V

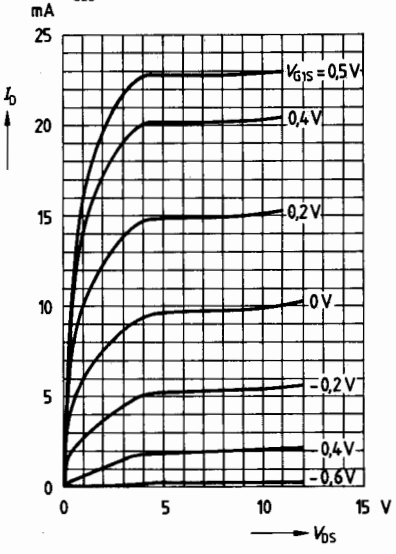
AC characteristics	Symbol	min.	typ.	max.	Unit
Forward transconductance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V f = 1 kHz	g_{fs}	–	24	–	mS
Gate 1 input capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V f = 1 MHz	c_{g1ss}	–	2.1	–	pF
Gate 2 input capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V f = 1 MHz	c_{g2ss}	–	1.2	–	pF
Reverse transfer capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V f = 1 MHz	c_{dg1}	–	25	–	fF
Output capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V f = 1 MHz	c_{dss}	–	1.05	–	pF
Power gain (test circuit 1) V_{DS} = 8 V, I_D = 10 mA, f = 200 MHz, G_G = 2 mS, G_L = 0.5 mS, V_{G2S} = 4 V	G_{ps} –	–	28	–	dB
(Test circuit 2) V_{DS} = 8 V, I_D = 10 mA, f = 800 MHz, G_G = 3.3 mS, G_L = 1 mS, V_{G2S} = 4 V	–	–	20	–	dB

AC characteristics	Symbol	min.	typ.	max.	Unit
Noise figure (test circuit 1) V_{DS} = 8 V, I_D = 10 mA, f = 200 MHz, G_G = 2 mS, G_L = 0.5 mS, V_{G2S} = 4 V	F	–	0.6	–	dB
(test circuit 2) V_{DS} = 8 V, I_D = 10 mA, f = 800 MHz, G_G = 3.3 mS, G_L = 1 mS, V_{G2S} = 4 V		–	1	–	dB
Control range (test circuit 2) V_{DS} = 8 V, V_{G2S} = 4 ... –2 V f = 800 MHz	ΔG_{ps}	40	–	–	dB

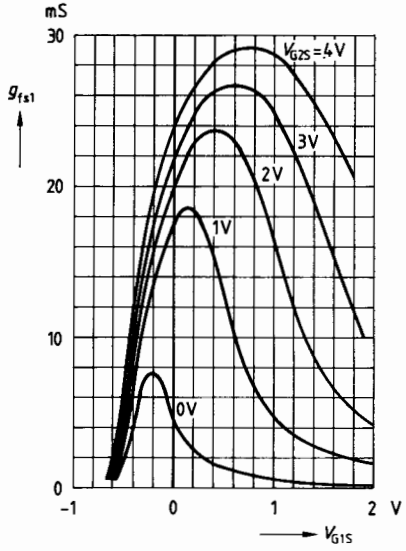
Total power dissipation $P_{tot} = f(T_A)$



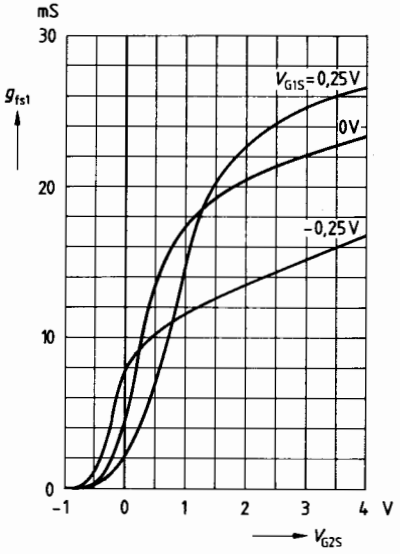
Output characteristics $I_D = f(V_{DS})$
V_{G2S} = 4 V



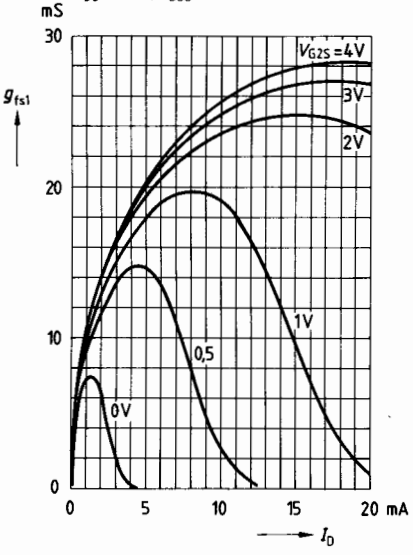
Gate 1 forward transconductance
$g_{fs1} = f(V_{G1S})$
V_{DS} = 8 V, I_{DSS} = 10 mA, f = 1 kHz



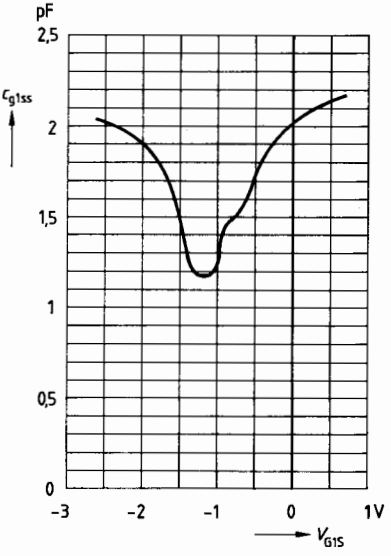
Gate 1 forward transconductance
$g_{fs1} = f(V_{G2S})$
V_{DS} = 8 V, I_{DSS} = 10 mA, f = 1 kHz



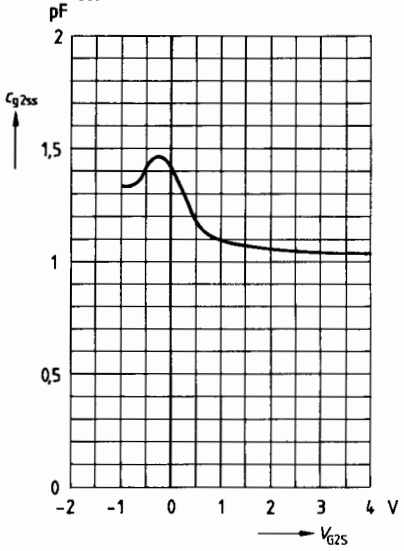
Gate 1 forward transconductance
$g_{fs1} = f(I_D)$
V_{DS} = 8 V, I_{DSS} = 10 mA, f = 1 kHz



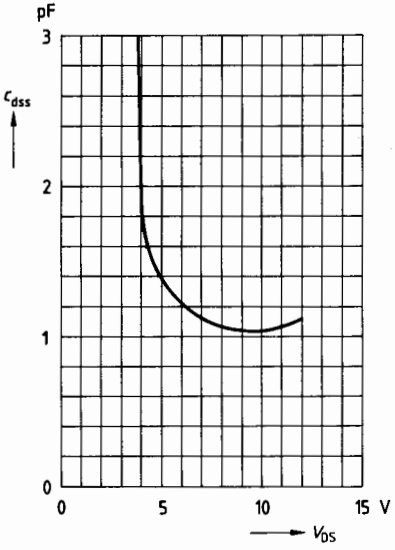
Gate 1 input capacitance $c_{g1ss} = f(V_{G1S})$
V_{G2S} = 4 V, V_{DS} = 8 V, I_{DSS} = 10 mA
f = 1 MHz



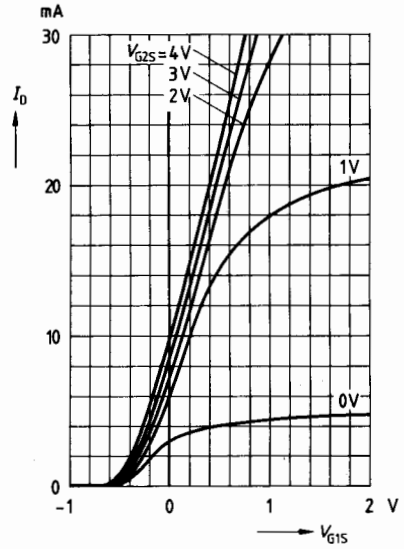
Gate 2 input capacitance $c_{g2ss} = f(V_{G2S})$
$V_{G1S} = 0$, $V_{DS} = 8$ V
$I_{DSS} = 10$ mA, $f = 1$ MHz



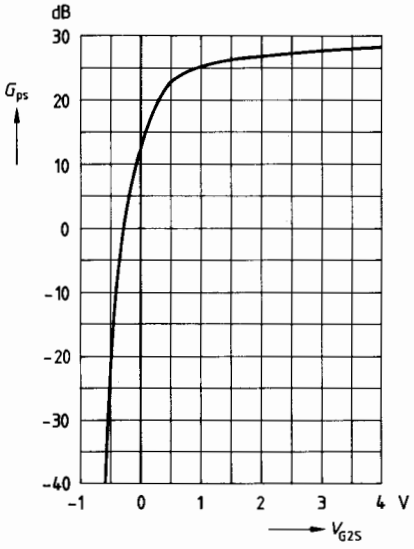
Output capacitance $c_{dss} = f(V_{DS})$
$V_{G1S} = 0$, $V_{G2S} = 4$ V
$I_{DSS} = 10$ mA, $f = 1$ MHz



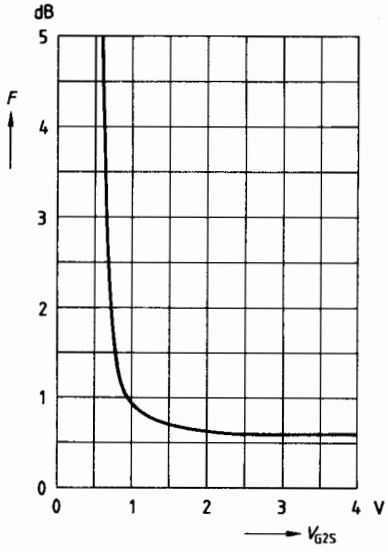
Drain current $I_D = f(V_{G1S})$
$V_{DS} = 8$ V



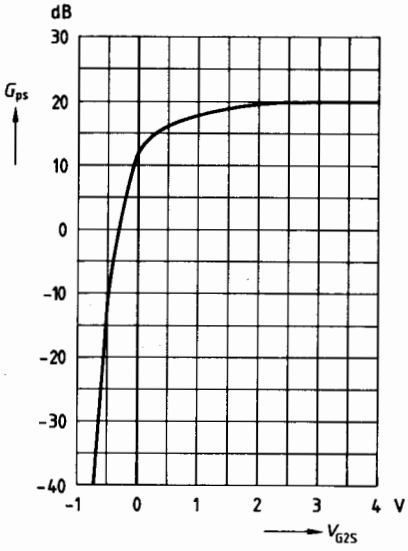
Power gain $G_{ps} = f(V_{G2S})$
$V_{DS} = 8$ V, $V_{G1S} = 0$
$I_{DSS} = 10$ mA, $f = 200$ MHz
(s. test circuit 1)



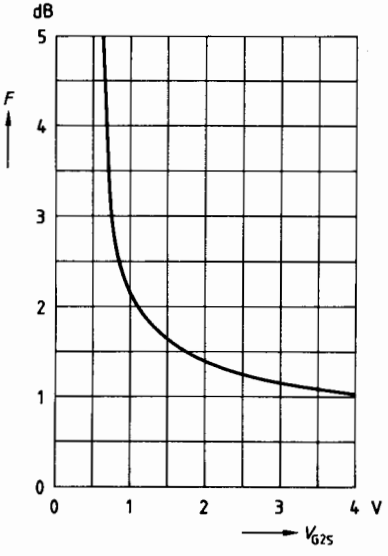
Noise figure $F = f(V_{G2S})$
V_{DS} = 8 V, V_{G1S} = 0, I_{DSS} = 10 mA,
f = 200 MHz, (s. test circuit 1)



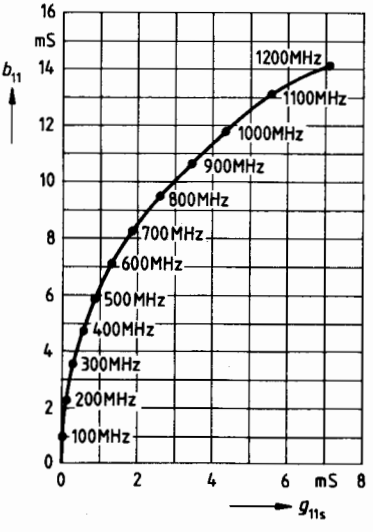
Power gain $G_{ps} = f(V_{G2S})$
V_{DS} = 8 V, V_{G1S} = 0, I_{DSS} = 10 mA,
f = 800 MHz, (s. test circuit 2)



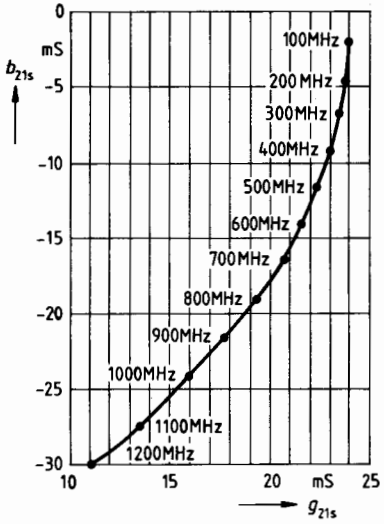
Noise figure $F = f(V_{G2S})$
V_{DS} = 8 V, V_{G1S} = 0, I_{DSS} = 10 mA,
f = 800 MHz, (s. test circuit 2)



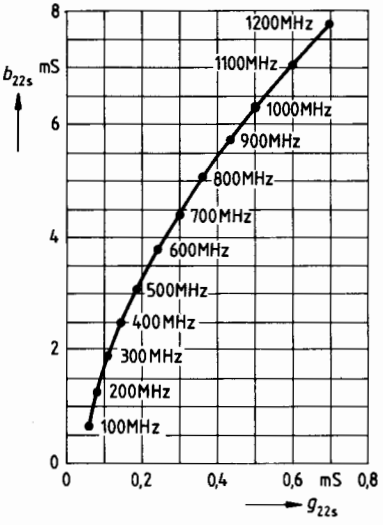
Gate 1 input admittance y_{11s}
V_{DS} = 8 V, V_{G2S} = 4 V, V_{G1S} = 4 V,
I_{DSS} = 10 mA, (common source)



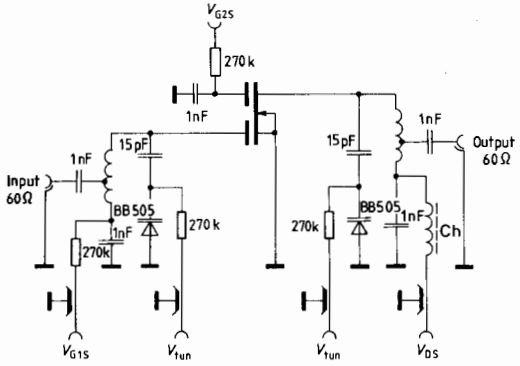
Gate 1 forward transfer admittance y_{21s}
V_{DS} = 8 V, V_{G2S} = 4 V, V_{G1S} = 0
I_{DSS} = 10 mA, (common source)



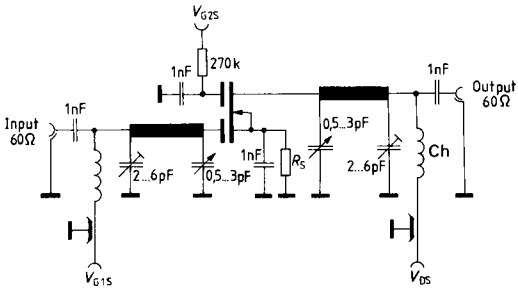
Output admittance y_{22s}
V_{DS} = 8 V, V_{G2S} = 4 V, V_{G1S} = 0
I_{DSS} = 10 mA, (common source)



Test circuit 1, power gain and noise figure
f = 200 MHz, G_G = 2 mS, G_L = 0.5 mS



Test circuit 2, power gain and noise figure
f = 800 MHz, G_G = 3.3 mS, G_L = 1 mS



Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation, Balanstraße 73, D-8000 München 80.