HEWLETT hp PACKARD
COMPONENTS

MICROWAVE GaAs FETS

NEW

2N6680 (HFET-1101) HFET-1102

Features

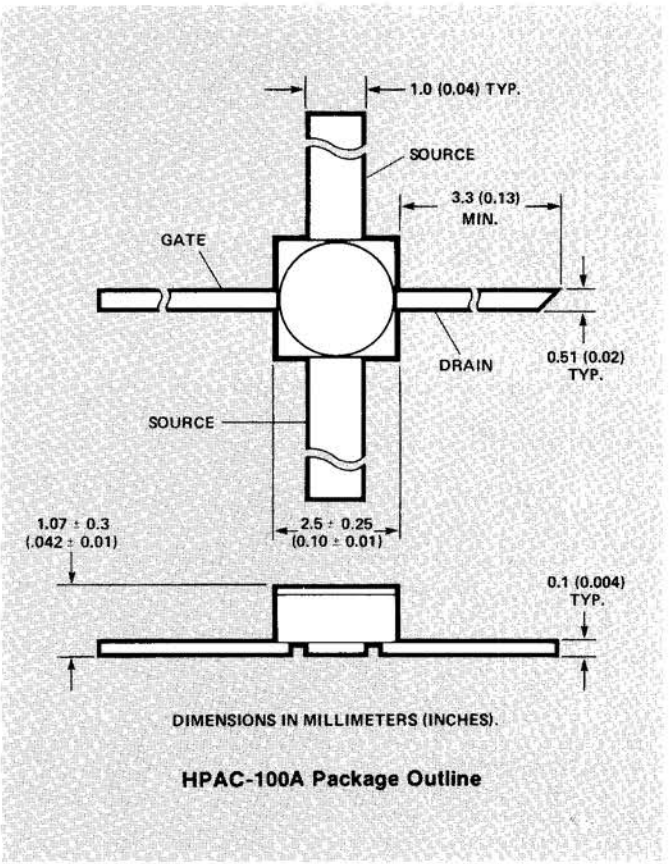
LOW NOISE FIGURE
- **1.6 dB Typical at 4 GHz (2N6680)**
- **1.7 dB Maximum at 4 GHz (HFET-1102)**
- **1.5 dB Typical**

HIGH GAIN
- **16 dB Typical at 4 GHz**

HIGH OUTPUT POWER
- **15.5 dBm Typical Linear Power Output at 4 GHz**

USABLE TO 12 GHz

RUGGED HERMETIC PACKAGE



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100A Package Outline

Description/Applications

The 2N6680 (HFET-1101) and the HFET-1102 are gallium arsenide Schottky gate field effect transistors in a package suitable for narrow band operations to 12 GHz. Their superior microwave performance in noise figure and gain make them useful for applications such as land and satellite communications, and radar.

2N6680 (HFET-1101) and HFET-1102 are supplied in the HPAC-100A, a rugged metal/ceramic hermetic package, and are capable of meeting the requirements of MIL-S-19500.

The HFET-1102 is a low noise and gain selection of the 2N6680.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, V_{DS} = 4.0V, V_{GS} = 0V		mA	40		120
V_{GSP}	Pinch Off Voltage, V_{DS} = 4.0V, I_{DS} = 100 μA		V	-1.5		-5.0
g_m	Transconductance, V_{DS} = 4.0V, ΔV_{GS} = 0V to -0.5V		mmho	30	40	
$G_{a(max)}$	Maximum Available Gain V_{DS} = 4.0V, V_{GS} = 0	f = 4 GHz	dB		16	
F_{MIN}	Noise Figure 2N6680: HFET-1102:	f = 4 GHz 4 GHz	dB		1.6 1.4	2.2 1.7
G_a	Associated Gain 2N6680: HFET-1102: V_{DS} = 3.5V, I_{DS} = 15% I_{DSS} (Typ. 12 mA)	f = 4 GHz 4 GHz	dB	9.5 11.0	11.0 12.0	
P_{1dB}	Power at 1 dB Compression, V_{DS} = 5.0V, I_{DS} = 50% I_{DSS} Tuned for Maximum Output Power at +5 dBm Input	f = 4 GHz 8 GHz	dBm		15.5 14.0	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-5.0V \leq V_{GS} \leq 0.0V$	5V
$V_{GS[2]}$	Gate to Source Voltage $5.0V \geq V_{DS} \geq 0.0V$	-5V
$T_{CH[3]}$	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 150°C (assumed Activation Energy = 1.6 eV). Corresponds to Maximum Ratings for 2N6680.
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. θ_{jc} — Thermal resistance, channel to case = 200°C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-10V \leq V_{GS} \leq 0.0V$	11V
$V_{GS[2]}$	Gate to Source Voltage $10.0V \geq V_{DS} \geq 0.0V$	-10V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
Lead Soldering Temperature[3] 250°C for 10 sec. each lead.		

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward Gate Current should not exceed 3 mA.
3. See Handling and Use Precautions. (page 13).

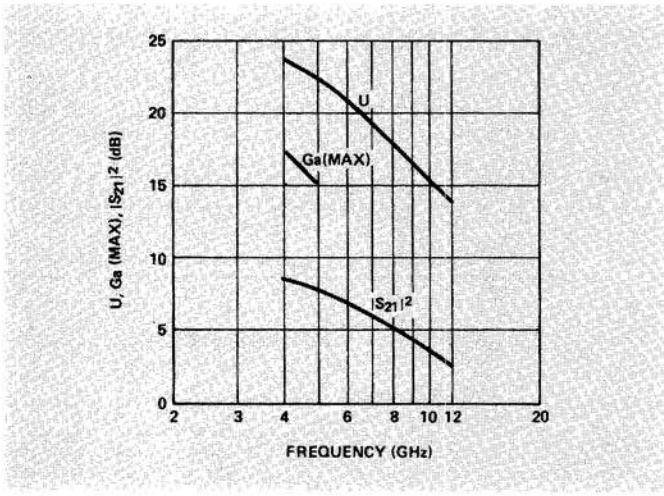


Figure 1. Typical Mason's Gain (U), $G_{a\ (max)}$, and $|S_{21}|^2$ vs. Frequency at V_{DS} = 4.0V, I_{DS} = 100% I_{DSS}.

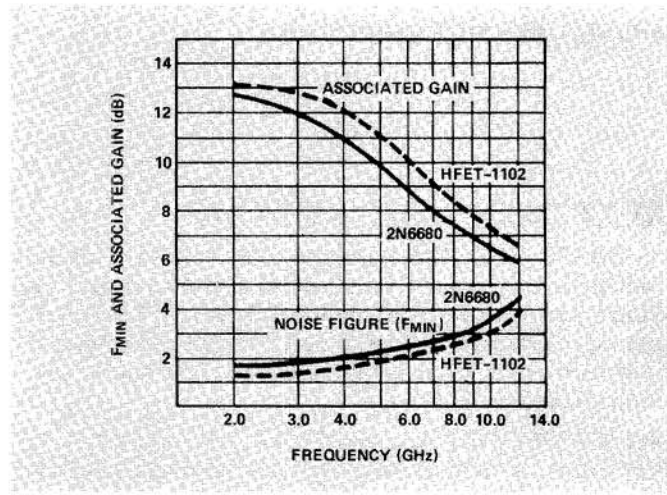


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency. V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

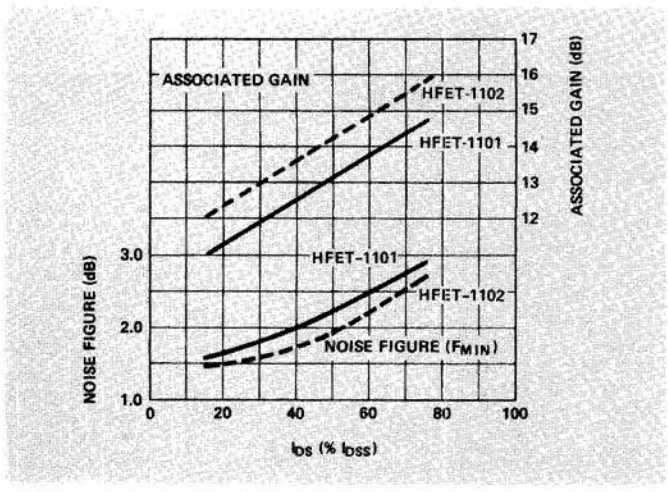


Figure 3. Typical Noise Figure and Associated Gain vs. Drain Current (I_{DS}) at 4 GHz, V_{DS} = 3.5V.

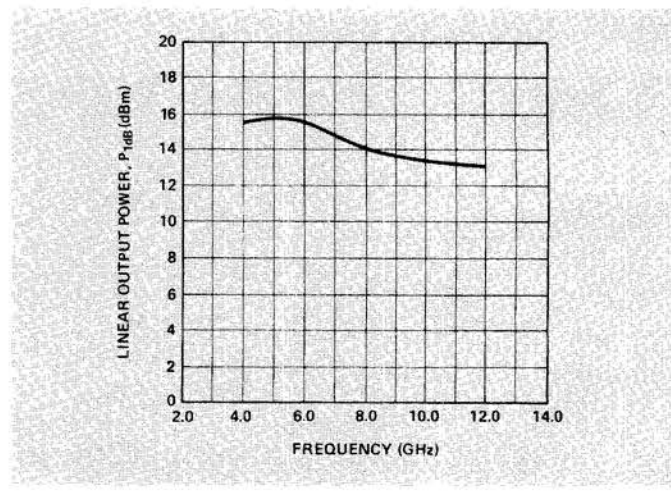


Figure 4. Typical Output Power at 1 dB Compression vs. Frequency. V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}. Tuned for Maximum Output Power at +5 dBm Input.

Typical S-Parameters

High Gain Bias: V_{DS} = 4.0V, V_{GS} = 0V

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.894	-60.6	3.122	123.6	.020	62.4	.781	-27.6
3.0	.801	-88.9	2.863	98.9	.025	55.8	.755	-40.5
4.0	.720	-116.2	2.597	75.6	.028	56.7	.732	-54.0
5.0	.662	-142.2	2.391	53.8	.034	62.0	.723	-67.7
6.0	.614	-167.4	2.187	32.4	.046	65.0	.716	-83.0
7.0	.588	169.3	1.985	12.1	.061	61.6	.711	-100.1
8.0	.580	148.1	1.807	-7.2	.083	54.8	.708	-118.2
9.0	.585	128.9	1.650	-25.6	.103	40.4	.720	-136.5
10.0	.593	110.9	1.535	-43.9	.121	31.1	.744	-155.5
11.0	.589	94.0	1.433	-62.6	.145	17.9	.765	-174.3
12.0	.574	76.6	1.329	-81.9	.164	2.4	.779	167.0

Linear Power Bias: V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.912	-57.8	2.836	125.2	.033	56.3	.705	-29.2
3.0	.829	-87.2	2.668	99.7	.044	41.7	.662	-43.7
4.0	.750	-116.5	2.458	74.5	.050	30.2	.632	-59.3
5.0	.683	-144.1	2.259	51.1	.054	21.5	.610	-76.3
6.0	.641	-171.3	2.053	28.5	.057	16.3	.572	-95.7
7.0	.625	164.1	1.847	6.3	.061	13.6	.556	-115.1
8.0	.621	142.7	1.664	-14.0	.069	9.8	.554	-133.0
9.0	.626	124.9	1.510	-33.1	.080	3.5	.589	-155.0
10.0	.627	108.4	1.382	-51.3	.095	-3.7	.609	-175.8
11.0	.615	92.4	1.257	-70.1	.106	-14.4	.614	166.3
12.0	.598	76.6	1.155	-88.0	.123	-26.1	.624	150.6

Minimum Noise Figure Bias: V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.935	-51.9	2.166	128.3	.045	54.6	.733	-30.5
3.0	.862	-77.1	2.070	104.4	.060	39.3	.697	-45.4
4.0	.792	-102.4	1.955	81.1	.070	26.0	.659	-60.8
5.0	.733	-127.2	1.860	58.7	.074	14.8	.630	-76.0
6.0	.674	-152.0	1.740	36.4	.075	6.2	.600	-92.6
7.0	.631	-175.5	1.599	15.2	.074	1.3	.578	-110.8
8.0	.607	162.8	1.469	-4.4	.077	.5	.565	-129.5
9.0	.601	143.0	1.352	-23.4	.087	-6.2	.570	-148.4
10.0	.602	124.5	1.261	-41.8	.091	-10.3	.585	-167.6
11.0	.594	107.3	1.180	-60.5	.104	-16.4	.600	173.5
12.0	.575	90.0	1.101	-79.5	.119	-27.0	.613	154.6

Typical Noise Parameters[1]

2N6680 (HFET-1101) and HFET-1102

Frequency (GHz)	Γ_o		$\Gamma_L = [S'_{22}]^*$		F_{MIN} (dB)	R_N (Ohms)
	Mag.	Ang.	Mag.	Ang.		
2.0	.730	60°	.829	44°	1.25	19.40
4.0	.618	98°	.656	75°	1.60	23.14
6.0	.575	138°	.601	104°	2.20	6.64
8.0	.617	-170°	.644	137°	2.80	1.88
10.0	.610	-128°	.693	-170°	3.60	25.47
12.0	.660	-87°	.749	-157°	4.50	49.10

Note:
1. Optimum Input Reflection Coefficient (Γ_o) Output Match for Minimum Noise (Γ_L), Associated Noise Figure (F_{MIN}) and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

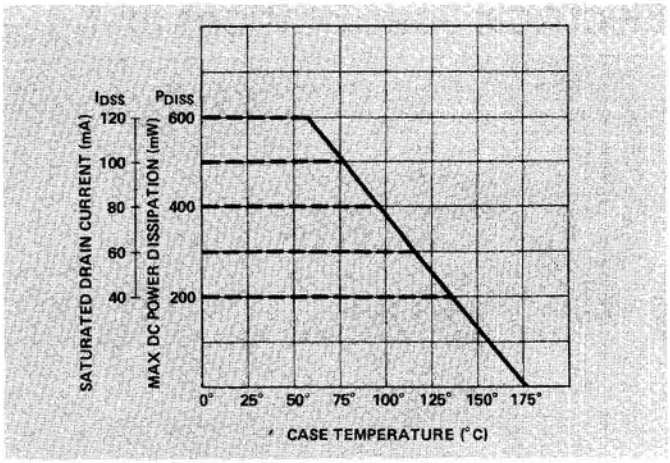


Figure 5. P_{DISS} vs. Temperature, Power Derating Curve at V_{DS} = 5V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with solid diagonal line.