

## Differential Output PLL Clock Generator

### Description

The **ICS1561A** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS's advanced CMOS mixed mode technology, the **ICS1561A** provides a low cost solution for high-end video clock or Teleclock™ generation.

The **ICS1561A** has differential clock outputs (CLK and CLK\*) that are compatible with industry standard video DACs & RAMDACs™. Additional clock outputs, FDIV2, FDIV4 and FDIV8, provide frequencies which are 1/2, 1/4 and 1/8 the main clock frequency.

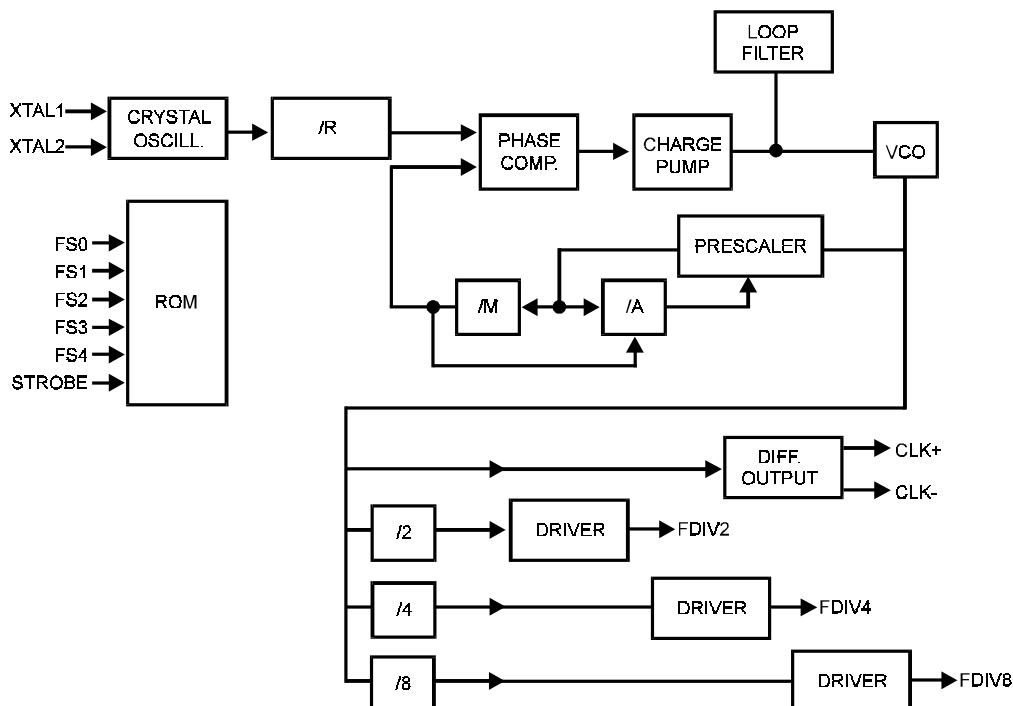
Operating frequencies are selectable from a preprogrammed (customer defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1561A**.

The **ICS1561A-728** is an excellent low-jitter 155.52 MHz Teleclock source for communications systems. When addressed at 19<sub>10</sub> (13 hex) with a 19.44 MHz reference, the **ICS1561A-728** provides an STS-3 (STM-1) differential clock that is compatible with SONET and ATM transmitters.

### Features

- High Frequency operation for extended video modes - up to 230 MHz
- Compatible with Brooktree high performance RAMDACs
- Low Cost - Eliminates need for multiple ECL crystal clock oscillators in video display subsystems
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity provides optimized loop gain over entire frequency range
- Strobed/Transparent frequency select options
- Small footprint - 20-pin DIP or SOIC packages available
- Fully backward compatible to ICS1561
- -728 option capable of STS-3/STM-1 communication clock generation

### Block Diagram

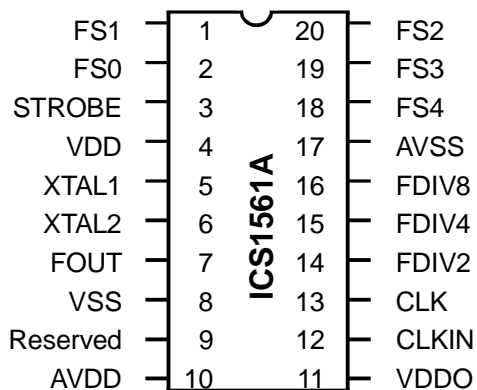


RAMDAC is a trademark of Brooktree Corporation.  
Teleclock is a trademark of Integrated Circuit Systems, Inc.



# ICS1561A

## Pin Configuration



**20-Pin DIP or SOIC**

## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS1		Frequency select input, TTL compatible.
2	FS0		Frequency select input, TTL compatible (LSB).
3	STROBE		Negative edge clock for select inputs, TTL compatible.
4	VDD		5V power pin.
5	XTAL1		Crystal interface/Ext. oscillator input.
6	XTAL2		Crystal interface.
7	FOUT		Clock output, TTL compatible.
8	VSS		Digital ground.
9	Phase-out		Phase comparator output.
10	AVDD		Analog VDD input.
11	VDDO		Output stage VDD supply pin.
12	CLOCKN		Complementary clock output, positive ECL.
13	CLOCK		Clock output, positive ECL.
14	FDIV2		Clock/2 output, TTL compatible.
15	FDIV4		Clock/4 output, TTL compatible.
16	FDIV8		Clock/8 output, TTL compatible.
17	AVSS		Analog ground.
18	FS4		Frequency select input, TTL compatible.
19	FS3		Frequency select input, TTL compatible.
20	FS2		Frequency select input, TTL compatible.



## Absolute Maximum Ratings

Supply voltage . . . . .	V <sub>DD</sub> . . . . .	-0.5V to +7V
Ambient operating temp . . . . .	T <sub>O</sub> . . . . .	0°C to 70°C
Storage temperature . . . . .	T <sub>S</sub> . . . . .	-85°C to +150°C
Input Voltage . . . . .	V <sub>IN</sub> . . . . .	-0.5V to V <sub>DD</sub> +0.5V
Output Voltage . . . . .	V <sub>OUT</sub> . . . . .	-0.5V to V <sub>DD</sub> +0.5V
Clamp Diode Current . . . . .	V <sub>IK</sub> & I <sub>OK</sub> . . . . .	±30mA
Output Current per Pin . . . . .	I <sub>OUT</sub> . . . . .	±50mA
Power Dissipation . . . . .	P <sub>D</sub> . . . . .	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to >=V<sub>SS</sub> and <=V<sub>DD</sub>.

## DC Characteristics

(Power Supply Voltage 4.75-5.25 Volts)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V <sub>IL</sub>	V <sub>DD</sub> =5V	V <sub>SS</sub>		0.8	V
Input High Voltage	V <sub>IH</sub>	V <sub>DD</sub> =5V	2.0		V <sub>DD</sub>	V
Input Leakage Current	I <sub>IH</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-		10	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =8.0mA	-		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =4.0mA	2.4		-	V
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> =5V	-		30	mA
Internal Pull-up Current	R <sub>UP</sub>	V <sub>DD</sub> =5V	25		100	μA
Input Pin Capacitance	C <sub>IN</sub>	F <sub>C</sub> =1MHz	-		8	pF
Output Pin Capacitance	C <sub>OUT</sub>	F <sub>C</sub> =1MHz	-		12	pF



# ICS1561A

## Circuit Description

### Overview

The **ICS1561A** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1561A** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

### Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1561A**. The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1561A** is powered-up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

### Divided Dot clock Outputs

The **ICS1561A** has additional outputs which provide a /2, /4 and /8 of the main frequency.

### Output Stage Description

The CLK and  $\overline{\text{CLK}}$  outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and clock\* of a RAMDAC device when a resistive network is utilized.

The divided outputs are high current CMOS type drives.

### Frequency Synthesizer Description

The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1561A** from an external frequency source.

The **ICS1561A** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase frequency detector to be matched in frequency and phase. This occurs when:

$$F_{(\text{VCO})} = \frac{F(\text{XTAL1}) * \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers). The divider programming is one of the functions performed by the ROM lookup table in the **ICS1561A**. The VCO gain is also ROM programmable which permits the **ICS1561A** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post divider may be inserted between the VCO and the CLK and  $\overline{\text{CLK}}$  outputs of the **ICS1561A**. This is useful in generation of lower frequencies, as the VCO has been optimized for high frequency operation. Different post divider settings may be used for each frequency in the table.



## Application Information

### *Power Supplies*

The **ICS1561A** has a VDDO pin which is the supply of +5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1561A**.

The AVDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to “track” through power supply fluctuations without visible effects.

### **Crystal Oscillator and Crystal Selection**

The **ICS1561A** has circuitry onboard to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti (also called parallel) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series resonant crystals may also be used with the **ICS1561A**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.0050.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1561A** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

### **Bus Clock Interface**

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (5) and keep the lead length of the capacitor to XTAL1 (5) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1561A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (6) must be left open in this configuration.

### **ICS1561A Interface**

The **ICS1561A** should be located as close as possible to the video DAC or RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion. CLK and  $\overline{\text{CLK}}$  connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.



# ICS1561A

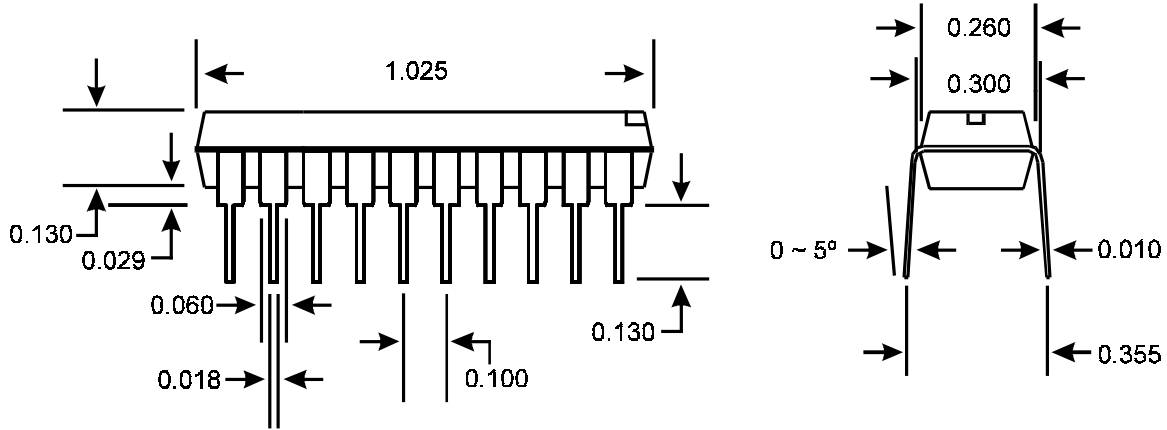
## ICS1561A Standard Patterns

ICS produces standard frequency patterns for the **ICS1561A**. These patterns include the majority of frequencies most customers require. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS1561A-706	ICS1561A-707	ICS1561A-723	ICS1561A-724	ICS1561A-725	ICS1561A-726	ICS1561A-727	ICS1561A-728
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	12.273	25.144	100.227	100.227	150.340	87.954	119.999	20.045
1	14.560	28.188	104.999	101.911	151.772	80.181	124.090	24.971
2	15.619	32.454	109.963	104.132	154.285	66.818	132.167	30.000
3	25.199	36.060	115.387	106.123	155.590	60.000	136.022	35.000
4	27.862	37.447	119.999	108.181	158.454	49.943	139.999	40.090
5	30.320	39.841	124.958	109.963	160.363	10.090	143.999	44.999
6	31.500	44.822	130.024	111.860	162.272	32.005	147.954	49.943
7	38.571	57.272	135.104	113.703	163.636	24.080	151.772	54.981
8	43.388	64.145	139.999	115.847	165.893	43.977	155.590	59.999
9	50.400	65.082	145.090	117.914	167.999	40.090	160.363	64.982
A	50.664	72.344	149.999	120.000	169.970	33.409	163.636	69.999
B	51.244	74.454	154.636	122.255	171.818	30.000	168.000	74.895
C	54.981	76.363	160.363	124.090	173.553	24.971	171.818	80.181
D	57.272	80.181	164.945	125.999	175.909	20.045	175.909	84.985
E	62.999	84.401	169.970	128.021	178.181	150.000	179.999	89.999
F	64.010	98.181	174.832	130.024	179.999	160.363	183.933	95.215
10	68.727	100.227	179.999	132.167	182.045	169.970	188.181	99.886
11	75.170	107.386	184.704	133.917	183.933	180.000	191.505	104.999
12	88.111	107.807	190.431	136.022	186.136	190.431	196.363	109.963
13	99.272	110.139	194.727	137.975	188.181	200.454	199.772	114.545
14	99.272	111.449	200.454	140.000	190.431	209.999	203.823	119.999
15	100.227	129.818	204.976	141.880	191.505	219.927	208.264	124.958
16	111.531	134.759	209.999	144.000	193.772	230.775	212.245	129.965
17	125.999	139.999	214.772	146.197	196.363	240.000	216.363	134.999
18	139.999	160.363	219.927	147.954	198.545	249.917	219.927	139.999
19	160.363	169.328	225.511	150.340	200.454	259.930	223.721	144.971
1A	179.999	179.999	230.775	151.772	202.140	269.999	227.406	149.790
1B	200.454	200.454	235.119	154.285	203.823	279.999	231.694	154.896
1C	216.363	126.602	239.999	155.590	206.181	289.943	235.828	160.363
1D	59.999	128.021	245.454	158.454	208.264	299.580	239.999	164.945
1E	249.917	132.631	249.917	160.363	209.999	309.793	248.181	169.970
1F	7.860	136.636	255.123	162.272	212.245	PwrDwn	PwrDwn	174.832
Reference Frequency	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	14.31818 MHz	19.44 MHz

Note: All frequencies above 180 MHz in the standard patterns shown above are experimental and are not guaranteed.

Order info: ICS1561AM-XXX or ICS1561AN-XXX (M = SOIC pkg., N = DIP pkg., XXX = Pattern number)



20-Pin DIP Package

### Ordering Information

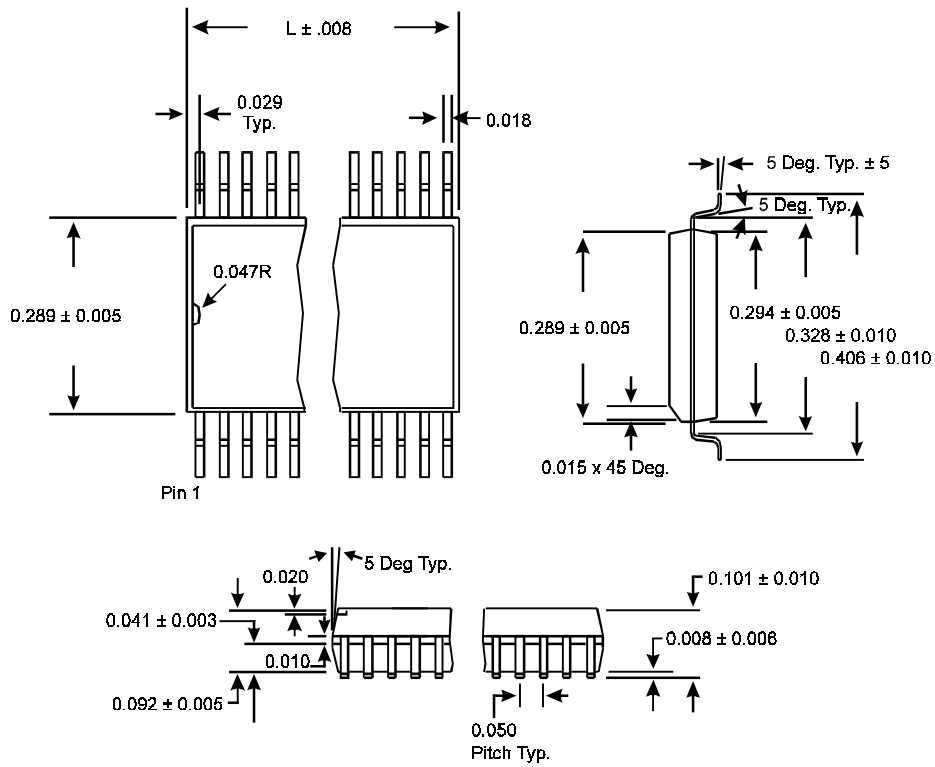
ICS1561AN-XXX

Example:

ICS XXXX N -XXX

- Prefix
  - Device Type (consists of 3 or 4 digit numbers)
  - Package Type  
N=DIP (Plastic)
  - Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- ICS, AV=Standard Device; GSP=Genlock Device

# ICS1561A



## SOIC Packages (wide body)

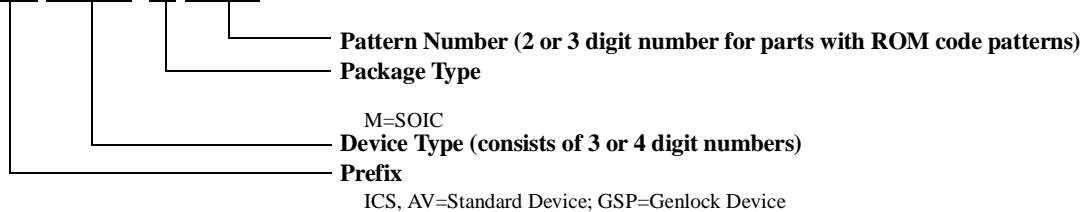
LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	0.354	0.404	0.454	0.504	0.604	0.704	0.804

## Ordering Information

### ICS1561AM-XXX

Example:

**ICS XXXX M -XXX**



PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.