ZERO BIAS SCHOTTKY DIODE MODEL FOR LOW POWER, MODERATE CURRENT RECTENNA

Jurianto Joe

Michael Chia Yan Wah

Ashok K. Marath

Ang Chip Hong
Centre for Wireless Communications

ABSTRACT : Zero bias Schottky diode model for low RF input power (≤ 0 dBm at antenna input port) and moderate DC current (≥ 30 μA) RECtifying anTENNAs (RECTENNAs) is investigated. The model provides diode parameters at the desired output DC current level to be matched with the antenna so that optimum power transfer from antenna to the diode occurs. The model relies primarily on DC V-I diode characteristic curve measurement results.

1. INTRODUCTION

A rectenna is a receiving antenna combined with a rectifying circuit which converts RF or microwave power into useful DC power. It can operate under both large and small signal (low power) conditions. In a large signal condition (≥ 10 dBm), the efficiency for a rectenna could achieve 80% - 90%. In a small signal condition (≤ 0 dBm), however, the efficiency is quite low since the diode is not fully operated in the forward bias and because of power dissipation in the diode.

This paper presents the experimental and simulation studies of zero bias Schottky diode model for low power, moderate current rectenna for passive tag RFID (Radio Frequency Identification) application. In certain RFID application, a rectenna is to supply certain output DC current and voltage to activate an Integrated Circuit (IC). The current state of the art low power CMOS IC would require a DC voltage supply of about 1 V and DC current of ≥ 30 μA for complex logical operations. Therefore, the issue is not only how efficient the rectenna is in converting RF to DC power, but also what the output DC voltage and current of the rectenna are at a certain RF input power level. An appropriate diode model that represents diode that rectifies desired DC output current level, will allow one to design a matching circuit to provide optimum power transfer from the antenna to the diode. The parameters for the diode model are obtained from measurement of the diode characteristic curve.

2. DIODE MODEL

Generally in RF design, a diode can be modeled as combination of resistance and capacitance. This is shown in Fig. 1 [1]. R_{pd} is the resistance of the barrier at the rectifying contact and varies with current flowing through it. It is large in the backward bias compared to that corresponding to the forward bias. It becomes smaller as the forward bias current increases. R_{sd} is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance. It dissipates RF energy as heat. C_j is junction capacitance arises from storage of charge in the boundary layer. Usually, only R_{sd} and C_j are provided in a component databook. R_{pd} is only given at certain operating current. Therefore, it is difficult to design matching circuit for this diode for operating current other than those given in the data book.

However, by applying DC voltage across the diode and measuring the DC current, one will be able to obtain the DC impedance of the diode $R_d(\omega=0)$ which is equivalent to the sum of R_{sd} and R_{pd} (see Fig. 1). Since R_{sd} is known, R_{pd} can be determined. Thus, by measuring diode V-I characteristic curve, one will be able to obtain R_{pd} for various diode DC current.

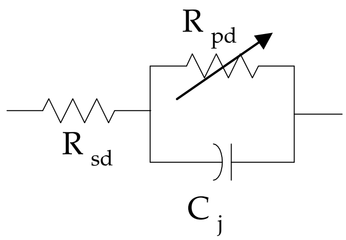

Fig. 1. Diode equivalent circuit.

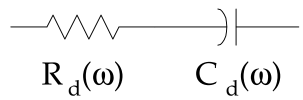

Fig. 2. S-parameter diode model.

The model shown in Fig.1 can be simplified further to that shown in Fig. 2. $R_d(\omega)$ and $C_d(\omega)$ in Fig. 2 can be related to the components in Fig. 1 by the following relations.

$$R_d(\omega) = R_{sd} + \frac{R_{pd}}{1+\omega^2 R_{pd}^2 C_j^2} \quad (1)$$

$$C_d(\omega) = C_j\left(1+\frac{1}{\omega^2 R_{pd}^2 C_j^2}\right) \quad (2)$$

ω is the desired operating frequency. Note that in the limit $R_{pd} \rightarrow \infty$, $C_d(\omega) \rightarrow C_j$ and $R_d(\omega) \rightarrow R_{sd}$. This occurs when the diode DC output current approaches zero. By providing matching circuit to the Schottky diode, utilizing diode model in Fig. 2, optimum power conversion efficiency can be achieved at the desired DC output current.

3. MODELING EXAMPLE : HSMS-8101 SCHOTTKY DIODE MODELING

From HP Communications Components data book [2], R_{sd} for HSMS-8101 is 4 Ω. C_j is 0.23 pF. R_{pd} as a function of diode current is obtained from the measured diode DC V-I characteristic curve. The resulting V-I curve is displayed in Fig. 3a. Figure 3b illustrates the dynamic resistance $R_d(\omega=0)$ versus diode current.

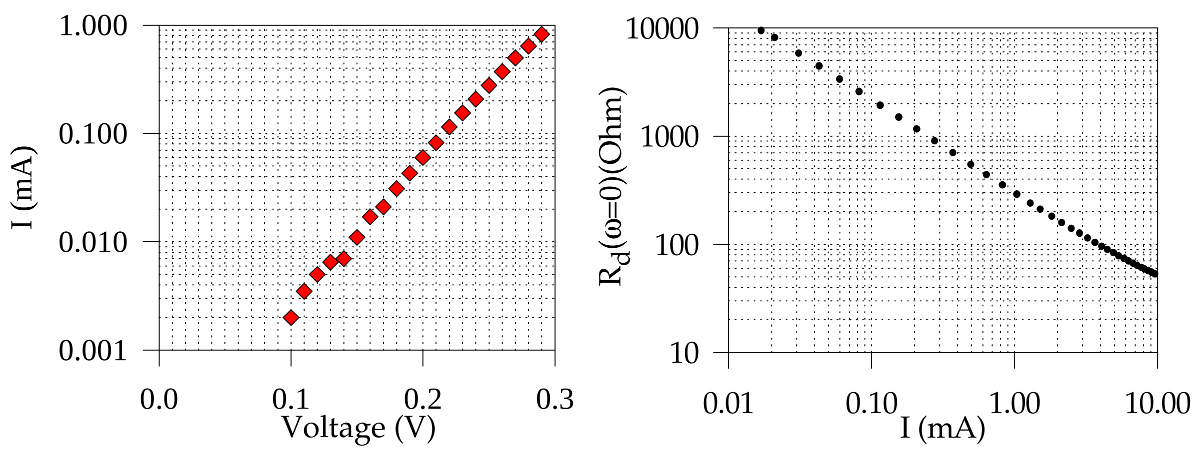

Fig. 3. Diode characteristic : (a) Measured diode DC V-I trace (b) $R_d(\omega=0)$ vs. diode current.

In our rectenna design, we are interested in 20 μA - 100 μA diode current range. The $R_d(\omega=0)$ (from Fig. 3b) ranges from 2 kΩ to 8 kΩ. For simplicity, we will use midpoint range $R_d(\omega=0)$. Since R_{pd} is much larger than R_{sd} in this current range, it is safe to assume that $R_{pd} \approx R_d(\omega=0)$. At midpoint, this is approximately equal to 5 kΩ. For 1.3 GHz operating frequency, by utilizing Eqs. (1) and (2) and the parameters obtained from data book and measurement, one should be able to get the equivalent $R_d(\omega)$ and $C_d(\omega)$ for a matching circuit design simulation purpose. For this case, $R_d(\omega) \approx 60$ Ω where R_{sd} has been taken into account, and $C_d(\omega) \approx 0.23$ pF. These values are utilized in the MDS to design matching circuit for the antenna to the diode.

4. RESULTS

The matching circuits for the diode was designed on FR-4. The dielectric constant ranged from 4.2 to 4.8. The loss tangent was 0.018 and the thickness was 0.78 mm (31 mils). The resonant frequency was 1.327 GHz and the matching circuit design was optimized using MDS. A sketch of the overall rectenna circuit equivalent is shown in Fig. 4. A variable load resistance R_L and a 1 nF short capacitance C were added to the rectenna circuit configuration to give the flexibility to control DC output current. V_{out} is a rectified DC voltage output.

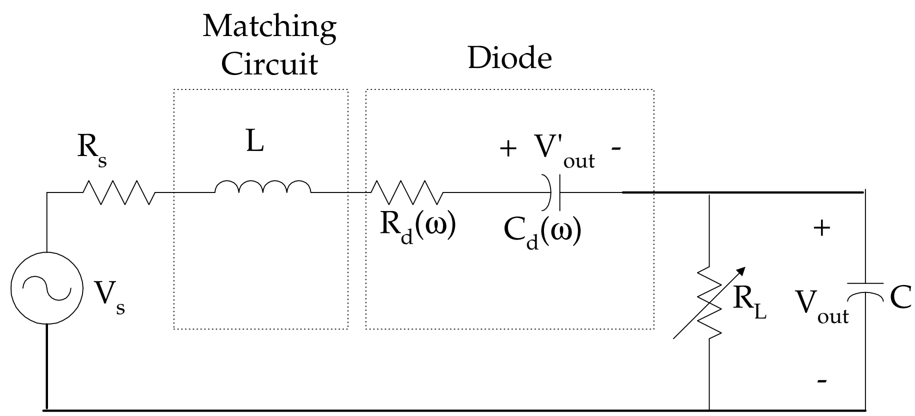

Fig. 4. Circuit representation of the rectenna circuit.

S_{11} of the rectenna rectifying circuit was obtained by connecting the rectifying circuit input port to the network analyzer. The frequency was swept from 1 GHz to 2 GHz. For RF to DC conversion measurement purpose, the signal was injected into the rectifying circuit by using signal generator. The input power was -10 dBm. The DC output voltage was measured across the load resistor. The load resistor was varied such that the current flowing through the load was between 20 μA - 100 μA.

Figure 5 illustrates the simulation and experimental S_{11} for 10 kΩ load resistor (The peak voltage at resonance was 0.45 V, hence the DC current was 45 μA). In the simulation, parasitic capacitance and inductance for the diode case was added to enhance accuracy. The simulation and experiment are in agreement. If the parasitic elements were not included in the simulation, the measured and simulation resonance would occur at different frequencies.

Figure 6 illustrates V_{out} versus frequency for different load resistance. Note that the peak voltage shifts to higher frequencies as the load resistance increases. This is due to R_{pd} variation as a function of current. As the load resistance increases, the DC current decreases which causes R_{pd} to increase. This virtually lower the capacitance value $C_d(\omega)$ and hence shifts the resonant frequency to higher values as the resonant frequency ω is related by

$$\omega = \frac{1}{\sqrt{LC_d(\omega)}} .$$

Figure 7 illustrates the performance of the rectenna at low power (≤ -10 dBm). The rectenna was placed 2.5 m away from the transmitter. The transmitting antenna gain was 7 dB. The input power to the transmitting antenna was varied from 0 - 20 dBm. P_r is the power available at the receiving rectangular patch antenna port which is connected to the rectifying circuit. 10 kΩ load was used for the measurement. At -10 dBm, the conversion efficiency is about 25%. The conversion efficiency drops below 10 % when the P_r is below -16 dBm.

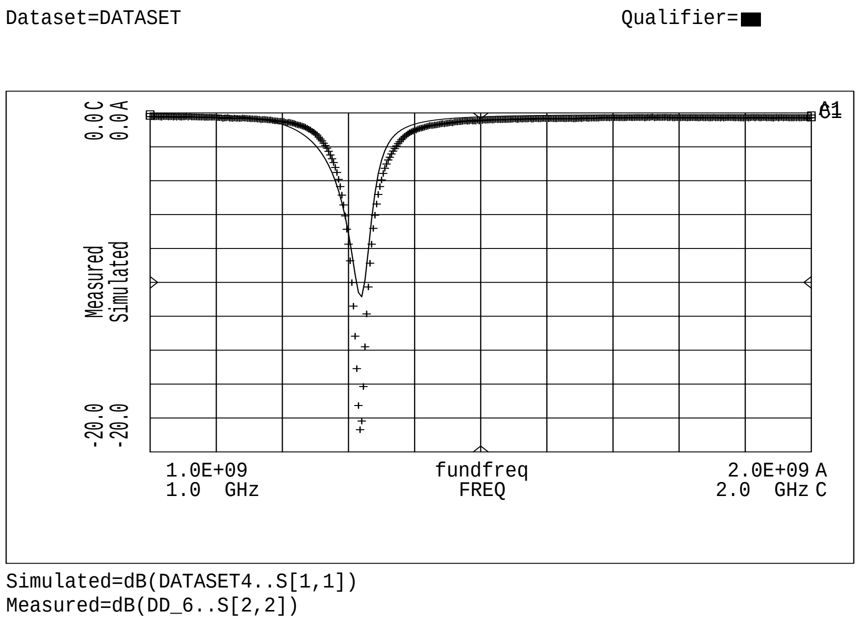

Fig. 5. S_{11} of the rectenna circuit with 10 kΩ load.

+ Measured

- Simulated

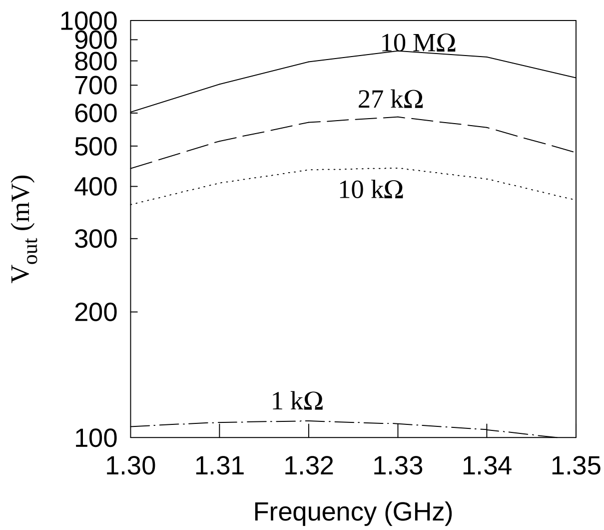

Fig. 6. V_{out} for various load resistance.

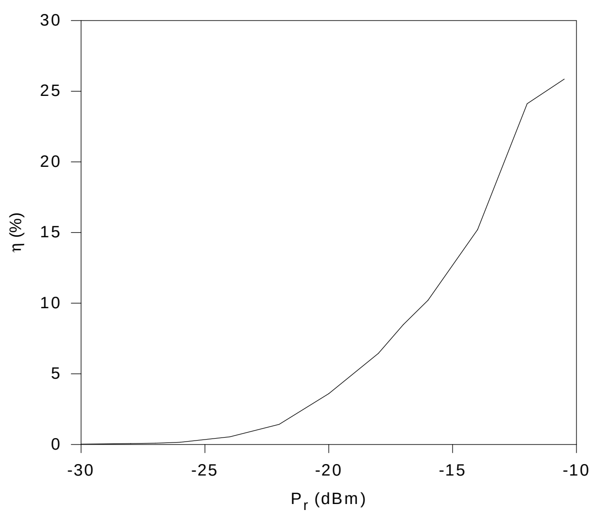

Fig. 7. Rectenna efficiency at various received power level.

5. SUMMARY

A diode model for low power, moderate current rectenna circuit is presented. The parameters of the diode model are obtained from the diode DC characteristic curve measurement. The model yields good agreements between MDS simulations and measurements. This model is useful in designing a rectenna circuit which can achieve optimum efficiency at the desired DC output current operation.

REFERENCES

1. H. C. Torrey and C. A. Whitmer, “Crystal Rectifiers,” *MIT Radiation Lab. Series*, no. 15, New York : McGraw Hill, 1948.

2. Hewlett Packard Data Book, “Communications Components, GaAs & Silicon Products,” pp. 3-63, 1993.

AUTHORS

Dr. Jurianto Joe received B.Sc. degree from University of Texas - Arlington in 1988, M.Sc. and Ph.D. degrees in Electrical Engineering from University of Wisconsin - Madison in 1990 and 1996, respectively. From 1991 to 1996, he was a research assistant in the High Power Millimeter Wave Laboratory at the University of Wisconsin and worked on moderate power, sheet beam compatible, rectangular grating TWT. Currently he is with Centre for Wireless Communications as a Member of Technical Staff. He is working on diode and circuit modeling for rectenna to be used in RFID tag. His research interests include multitone RF power amplifier, device modeling, and active antenna.

Dr. Michael Chia Yan Wah is a Member of Technical Staff and the project manager for Radio Frequency Identification Tracking (RFIT) project in the Centre of Wireless Communication (CWC). He is a MIEEE and graduated from Loughborough Univ.,UK, with a Ph.D. in 1994 and B.Sc. (1st Class Honours) in 1990. He has conducted the research on advanced antenna and radome systems for aerospace and satellite communication system in collaboration with British Aerospace Ltd, U.K. Currently, he is the manager responsible for the new technology focus group in RF, antenna and propagation in CWC. His research interest is in microstrip antenna, handset antenna, Frequency Selective Surface, electromagnetic techniques, Floquet’s Theorem, smart/adaptive antenna array, RFID system, propagation, linearisation of power amplifier.

Ashok K. Marath received his B.Tech. in Electronics Engineering from Regional Engineering College, Calicut in India. He worked as scientific officer in SAMEER, Bombay doing design of RF subsystems. Later he joined Indian Telephone Industries in Bangalore. He was involved in the development of digital microwave transmission equipment for six years. He joined PCI Ltd., Singapore in 1993 and was involved in the development of cellular and paging products. Currently he is the RF development manager responsible for RF subsystems in Centre for Wireless Communications.

Ang Chip Hong graduated with B.Eng. degree (Honours) in Electrical Engineering from NUS in 1996. He is a research engineer with Centre for Wireless Communications (CWC). His research interests are rectenna, microwave broadband power amplifiers and RF circuit design.