



# SL1640C & SL1641C

## DOUBLE BALANCED MODULATORS

The SL1640C and SL1641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL1640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL1641 has a single output designed as a current drive to a tuned circuit.

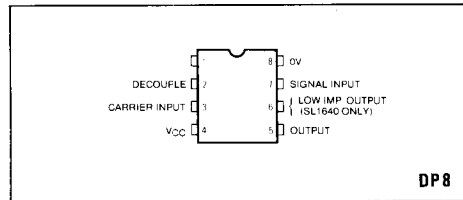


Fig. 1 Pin connections (top view)

### FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

### APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

### QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

### ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V  
Storage temperature:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

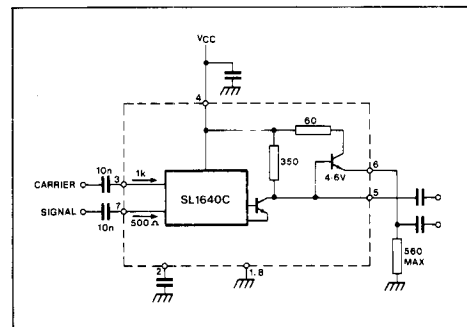


Fig. 2 Block diagram (SL1640C)

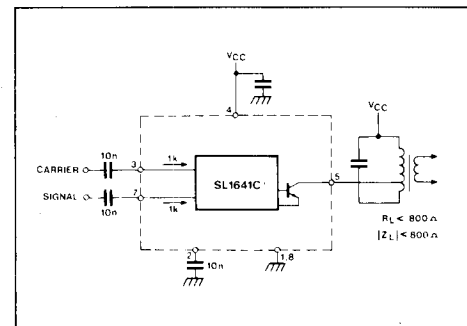


Fig. 3 Block diagram (SL1641C)

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage  $V_{CC}$ : 6VAmbient temperature:  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1640C		12	18	mA	
	SL1641C		10	15	mA	
Conversion gain	SL1640C	-3	0	+3	dB	
Conversion transconductance	SL1641C	1.7	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		k $\Omega$	
Signal input impedance	SL1640C		500		$\Omega$	
	SL1641C		1		k $\Omega$	
Maximum input voltage	SL1640C		210		mV rms	
	SL1641C		250		mV rms	
Signal leak	SL1640C	-30			dB	{ Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL1640C	-30			dB	
Signal leak	SL1641C	-18			dB	{ Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL1641C	-25			dB	
Intermodulation products	SL1640C		-45		dB	{ Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL1641C		-45		dB	
						{ Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier: 100mV rms, 28.25MHz Output: 2.75MHz

## APPLICATION NOTES

The SL1640C and SL1641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL1641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200 mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course, increases the gain of the circuit.

There are two outputs from the SL1640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 560 ohms to ground. The emitter

follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig. 4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

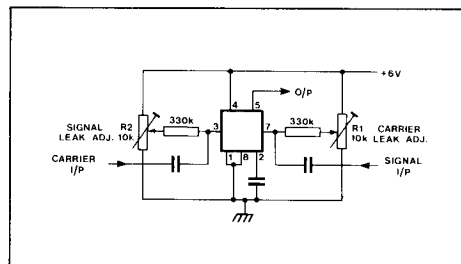


Fig. 4 Signal and carrier leak adjustment